TPS2041B, TPS2042B, TPS2043B, TPS2044B
TPS2051B, TPS2052B, TPS2053B, TPS2054B
SLVS514N – JUNE 2010 – REVISED JULY 2023

TPS20xxB Current-Limited, Power-Distribution Switches

1 Features

- 70-mΩ High-Side MOSFET
- 500-mA Continuous Current
- Thermal and Short-Circuit Protection
- Accurate Current Limit (0.75 A Minimum, 1.25 A Maximum)
- Operating Range: 2.7 V to 5.5 V
- 0.6-ms Typical Rise Time
- Undervoltage Lockout
- Deglitched Fault Report ($\overline{OC}$)
- No $\overline{OC}$ Glitch During Power Up
- Maximum Standby Supply Current: 1-µA (Single, Dual) or 2-µA (Triple, Quad)
- Ambient Temperature Range: –40°C to 85°C
- UL Recognized, File Number E169910
- Additional UL Recognition for TPS2042B and TPS2052B for Ganged Configuration

2 Applications

- Heavy Capacitive Loads
- Short-Circuit Protections

3 Description

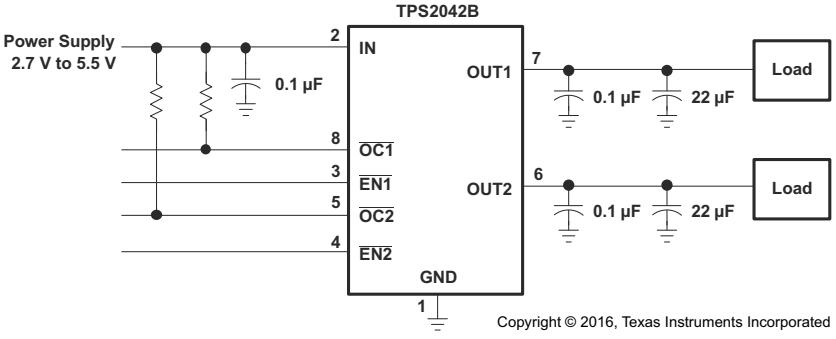
The TPS20xxB power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A (typical).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS20xxB	SOIC (8)	4.90 mm × 3.91 mm
	SOIC (16)	9.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	HVSSOP (8)	3.00 mm × 3.00 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic

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4 Revision History

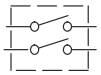
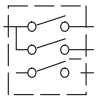
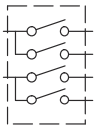
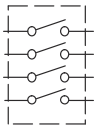
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (June 2016) to Revision N (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Update TPS2051BDBV and TPS2052BD electrical characteristics, including overcurrent trip threshold, high-level output supply current and undervoltage lockout	7
• Updated TPS2051BDBV and TPS2052BD Typical Characteristics	14
• Moved overcurrent description from Application and Implementation section to Detailed Description section	22
• Added TPS2051BDBV and TPS2052BD overcurrent description	22

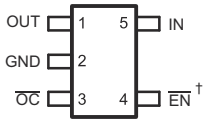
Changes from Revision L (June 2011) to Revision M (June 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	6

5 General Switch Catalog

GENERAL SWITCH CATALOG

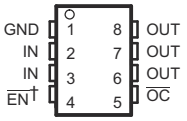
33 mΩ, Single	80 mΩ, Single	80 mΩ, Dual	80 mΩ, Dual	80 mΩ, Triple	80 mΩ, Quad	80 mΩ, Quad
						
TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

6 Pin Configuration and Functions



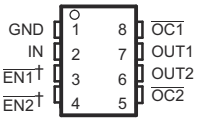
† All enable outputs are active high for the TPS205xB series.

Figure 6-1. TPS2041B and TPS2051B: DBV Package 5-Pin SOT-23 Top View



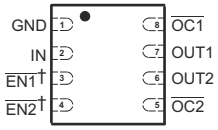
† All enable outputs are active high for the TPS205xB series.

Figure 6-2. TPS2041B and TPS2051B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View



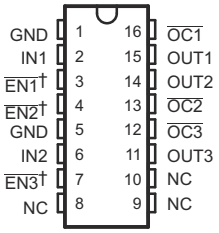
† All enable outputs are active high for the TPS205xB series.

Figure 6-3. TPS2042B and TPS2052B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View



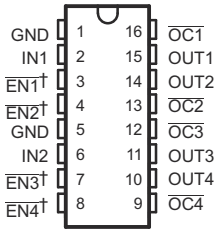
† All enable outputs are active high for the TPS205xB series.

Figure 6-4. TPS2042B and TPS2052B: DRB Package 8-Pin SON Top View



† All enable outputs are active high for the TPS205xB series.

Figure 6-5. TPS2043B and TPS2053B: D Package 16-Pin SOIC Top View



† All enable outputs are active high for the TPS205xB series.

Figure 6-6. TPS2044B and TPS2054B: D Package 16-Pin SOIC Top View

Table 6-1. Pin Functions (TPS2041B and TPS2051B)

NAME	PIN				I/O	DESCRIPTION
	TPS2041B	TPS2051B	TPS2041B	TPS2051B		
	SOIC AND DGN		SOT-23			
$\overline{EN}$	4	—	4	—	I	Enable input, logic low turns on power switch
EN	—	4	—	4	I	Enable input, logic high turns on power switch
GND	1	1	2	2	—	Ground
IN	2, 3	2, 3	5	5	I	Input voltage
$\overline{OC}$	5	5	3	3	O	Overcurrent open-drain output, active-low
OUT	6, 7, 8	6, 7, 8	1	1	O	Power-switch output

Table 6-2. Pin Functions (TPS2042B and TPS2052B)

PIN			I/O	DESCRIPTION
NAME	TPS2042B	TPS2052B		
	SOIC, HVSSOP, SON			
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN-OUT2
EN1	—	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1	—	Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
PowerPAD™	—	—	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin.

Table 6-3. Pin Functions (TPS2043B and TPS2053B)

PIN			I/O	DESCRIPTION
NAME	TPS2043B	TPS2053B		
	SOIC	SOIC		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	—	I	Enable input, logic low turns on power switch IN2-OUT3
EN1	—	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	—	7	I	Enable input, logic high turns on power switch IN2-OUT3
GND	1, 5	1, 5	—	Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3
NC	8, 9, 10	8, 9, 10	—	No connection
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

Table 6-4. Pin Functions (TPS2044B and TPS2054B)

PIN			I/O	DESCRIPTION
NAME	TPS2044B	TPS2054B		
	SOIC	SOIC		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	—	I	Enable input, logic low turns on power switch IN2-OUT3
$\overline{EN4}$	8	—	I	Enable input, logic low turns on power switch IN2-OUT4
EN1	—	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN1-OUT2

Table 6-4. Pin Functions (TPS2044B and TPS2054B) (continued)

PIN			I/O	DESCRIPTION
NAME	TPS2044B	TPS2054B		
	SOIC	SOIC		
EN3	—	7	I	Enable input, logic high turns on power switch IN2-OUT3
EN4	—	8	I	Enable input, logic high turns on power switch IN2-OUT4
GND	1, 5	1, 5	—	Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3 and OUT4
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent, open-drain output, active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{I(IN)}$, $V_{I(INx)}$	Input voltage (2)	–0.3	6	V
$V_{O(OUT)}$, $V_{O(OUTx)}$ (2)	Output voltage	–0.3	6	V
$V_{I(\overline{EN})}$, $V_{I(\overline{ENx})}$, $V_{I(EN)}$, $V_{I(ENx)}$	Input voltage	–0.3	6	V
$V_{I(/OC)}$, $V_{I(\overline{OCx})}$	Voltage range	–0.3	6	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current	Internally limited		
	Continuous total power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{I(IN)}$, $V_{I(INx)}$	Input voltage	2.7		5.5	V
$V_{I(\overline{EN})}$, $V_{I(\overline{ENx})}$, $V_{I(EN)}$, $V_{I(ENx)}$	Input voltage	0		5.5	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current	0		500	mA
T_J	Operating virtual junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2042xx and TPS2053xx					UNIT
		D (SOIC)		DBV (SOT-23)	DGN (HVSSOP)	DRB (SON)	
		8 PINS	16 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.3	81.6	208.6	53.6	47.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	42.7	122.9	58.7	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	39.1	37.8	35.5	14.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.3	10.4	14.6	2.7	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.1	38.8	36.9	35.3	14.2	°C/W

7.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS2042xx and TPS2053xx					UNIT
		D (SOIC)		DBV (SOT-23)	DGN (HVSSOP)	DRB (SON)	
		8 PINS	16 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	6.7	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 0.5 A, -40°C ≤ T_J ≤ 125°C		D and DGN packages		70	135	mΩ
				DBV package only		95	140	
	Static drain-source on-state resistance, 2.7-V operation	$V_{I(IN)}$ = 2.7 V, I_O = 0.5 A, –40°C ≤ T_J ≤ 125°C		D and DGN packages		75	150	mΩ
	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, I_O = 1 A, OUT1 and OUT2 connected, 0°C ≤ T_J ≤ 70°C		DGN package, TPS2042B/52B			49	mΩ
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 10 Ω	T_J = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V				0.4	1	
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V			0.05		0.5	
		$V_{I(IN)}$ = 2.7 V			0.05		0.5	
ENABLE INPUT $\overline{EN}$ AND $\overline{ENx}$								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V					0.8	V
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V			–0.5		0.5	µA
t_{on}	Turnon time	C_L = 100 µF, R_L = 10 Ω					3	ms
t_{off}	Turnoff time	C_L = 100 µF, R_L = 10 Ω					10	ms
CURRENT LIMIT								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit		T_J = 25°C	0.75	1	1.25	A
				–40°C ≤ T_J ≤ 125°C	0.7	1	1.3	
		$V_{I(IN)}$ = 5 V, OUT1 and OUT2 connected to GND, device enabled into short-circuit, measure at IN		0°C ≤ T_J ≤ 70°C TPS2042B/52B	1.5			
I_{OC} [2]	Overcurrent trip threshold	V_{IN} = 5 V, 100 A/s	TPS2041B TPS2051B (D and DGN packages only)		I_{OS}	1.5	1.9	A
			TPS2042B TPS2052B (DGN package only)		I_{OS}	1.55	2	
SUPPLY CURRENT (TPS2041B, TPS2051B)								
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	1	µA
				-40°°C ≤ T_J ≤ 125°C		0.5	5	

7.5 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	TPS2041B TPS2051B (D and DGN packages only)	T_J = 25°C		43	60	µA
			–40°C ≤ T_J ≤ 125°C		43	70	
		TPS2051BDBV	T_J = 25°C		75	95	
			–40°C ≤ T_J ≤ 125°C		75	95	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0		µA
SUPPLY CURRENT (TPS2042B, TPS2052B)							
Supply current, low-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V		T_J = 25°C		0.5	1	µA
			–40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V	TPS2042B TPS2052B (DGN package only)	T_J = 25°C		50	70	µA
			–40°C ≤ T_J ≤ 125°C		50	90	
		TPS2052BD	T_J = 25°C		95	120	uA
			–40°C ≤ T_J ≤ 125°C		95	120	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V		–40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, IN = ground		T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2043B, TPS2053B)							
Supply current, low-level output	No load on OUT, $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	2	µA
			–40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		65	90	µA
			–40°C ≤ T_J ≤ 125°C		65	110	
Leakage current	OUT connected to ground, $V_{I(ENx)}$ = 0 V		–40°C≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground		T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2044B, TPS2054B)							
Supply current, low-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	2	µA
			–40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		75	110	µA
			–40°C ≤ T_J ≤ 125°C		75	140	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		–40°C≤ T_J ≤ 125°C		1		µA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground		T_J = 25°C		0.2		µA
UNDERVOLTAGE LOCKOUT (All Devices excluding TPS2051BDBV and TPS2052BD)							
Low-level input voltage, IN, INx				2		2.5	V
Hysteresis, IN, INx	T_J = 25°C				75		mV
UNDERVOLTAGE LOCKOUT (TPS2051BDBV and TPS2052BD)							
Low-level input voltage, IN, INx				2		2.6	V
Hysteresis, IN, INx	T_J = 25°C				75		mV
OVERCURRENT $\overline{OC}$ and $\overline{OCx}$							
Output low voltage, $V_{OL(/OCx)}$	$I_{O(\overline{OCx})}$ = 5 mA					0.4	V
Off-state current	$V_{O(\overline{OCx})}$ = 5 V or 3.3 V					1	µA
$\overline{OC}$ deglitch	$\overline{OCx}$ assertion or deassertion			4	8	15	ms
THERMAL SHUTDOWN[3]							
Thermal shutdown threshold				135			°C

7.5 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
Recovery from thermal shutdown		125			°C
Hysteresis			10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) TPS2051BDBV and TPS2052BD don't have overcurrent trip threshold. Current will be limited to I_{OS} under different test conditon. Check Section 9.3.7 for more details.
(3) The thermal shutdown only reacts under overcurrent conditions.

7.6 Dissipation Ratings

PACKAGE	THERMAL RESISTANCE, θ_{JA}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN-8		1712.3 mW	17.123 mW/°C	941.78 mW	684.93 mW
D-8		585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW
D-16		898.47 mW	8.9847 mW/°C	494.15 mW	359.38 mW
DBV-5		285 mW	2.85 mW/°C	155 mW	114 mW
DRB-8 (Low-K)(1)	270 °CW	370 mW	3.71 mW/°C	203 mW	148 mW
DRB-8 (High-K)(2)	60 °CW	1600 mW	16.67 mW/°C	916 mW	866 mW

(1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note SLMA002 for further details.
(2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note SLMA002 for further details.

7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD)

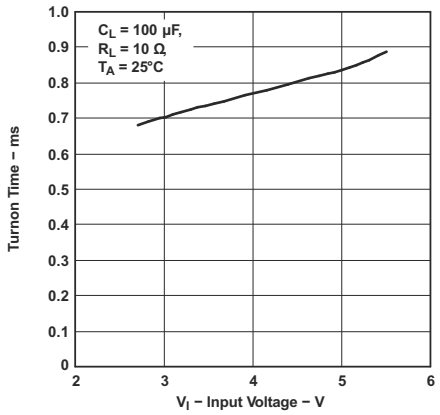


Figure 7-1. Turnon Time vs Input Voltage

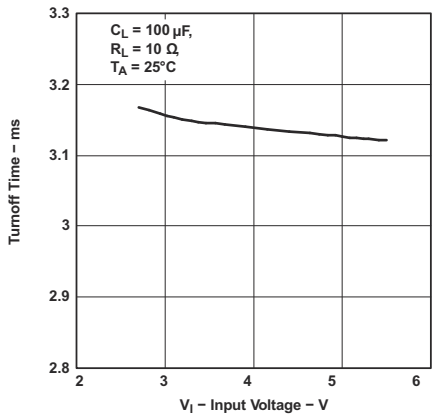


Figure 7-2. Turnoff Time vs Input Voltage