

Field Effect Transistor - Dual, N-Channel, Enhancement Mode



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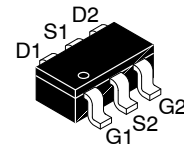
NDC7002N

General Description

These dual N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage applications requiring a low current high side switch.

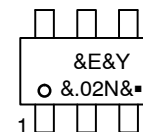
Features

- 0.51 A, 50 V, $R_{DS(ON)} = 2 \Omega @ V_{GS} = 10 \text{ V}$
- High Density Cell Design for Low $R_{DS(ON)}$
- Proprietary SUPERSOT™ -6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- High Saturation Current
- This is a Pb-Free Device



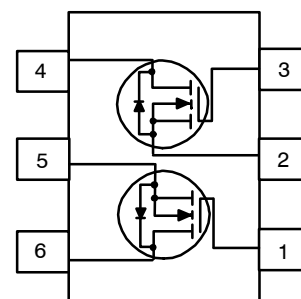
TSOT23 6-Lead
CASE 419BL

MARKING DIAGRAM



XXX = Specific Device Code
 &E = Space Designator
 &Y = Year of Production
 &. = Pin One Identifier
 ▪ = Pb-Free Package

PINOUT



SOT-6 (SUPERSOT™ -6)

ORDERING INFORMATION

Device	Package	Shipping†
NDC7002N	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NDC7002N

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	50	V
V_{GSS}	Gate-Source Voltage	20	V
I_D	Drain Current - Continuous (Note 1a) - Pulsed	0.51 1.5	A
P_D	Power Dissipation (Note 1a) (Note 1b) (Note 1c)	0.96 0.9 0.7	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	60	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	

NDC7002N

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain–Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	50			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40 V, V _{GS} = 0 V T _J = 125°C			1 500	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –20 V, V _{DS} = 0 V			–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA T _J = 125°C	1 0.8	1.9 1.5	2.5 2.2	V
R _{DS(ON)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 0.51 A T _J = 125°C		1 1.7	2 3.5	Ω
		V _{GS} = 4.5 V, I _D = 0.35 A		1.6	4	
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 10 V	1.5			A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 0.51 A		400		mS

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		20		pF
C _{oss}	Output Capacitance			13		pF
C _{rss}	Reverse Transfer Capacitance			5		pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = 25 V, I _D = 0.25 A, V _{GS} = 10 V, R _{GEN} = 25 Ω		6	20	ns
t _r	Turn–On Time			6	20	
t _{d(off)}	Turn–Off Delay Time			11	20	
t _f	Turn–Off Fall Time			5	20	
Q _g	Total Gate Charge	V _{DS} = 25 V, I _D = 0.51 A, V _{GS} = 10 V		1		nC
Q _{gs}	Gate–Source Charge			0.19		nC
Q _{gd}	Gate to Drain Charge			0.33		nC

DRAIN–SOURCE DIODE CHARACTERISTICS

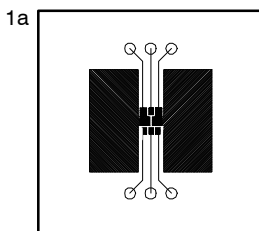
I _S	Maximum Continuous Source Current			0.51	A	
I _{SM}	Maximum Pulse Source Current (Note 2)			1.5	A	
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.51 A (Note 2)		0.8	1.2	V

1. R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

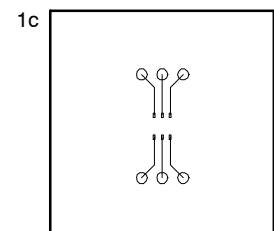
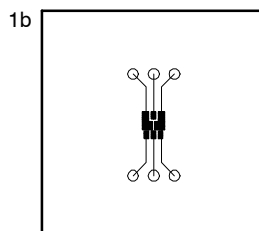
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)}@T_J$$

Typical R_{θJA} for single device operation using the board layouts shown below on 4.5"x5" FR–4 PCB in a still air environment:

- 130°C/W when mounted on a 0.125 in² pad of 2oz copper.
- 140°C/W when mounted on a 0.005 in² pad of 2oz copper.
- 180°C/W when mounted on a 0.0015 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



2. Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

TYPICAL ELECTRICAL CHARACTERISTICS

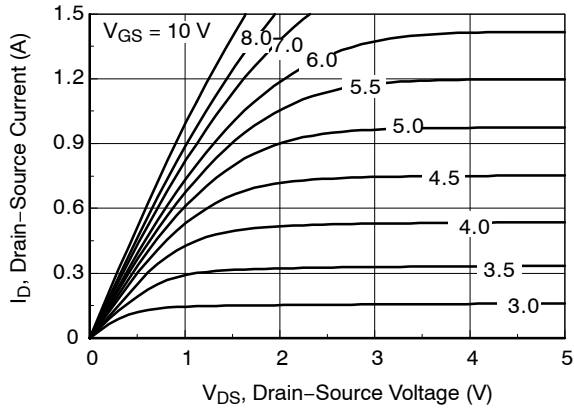


Figure 1. On-Region Characteristics

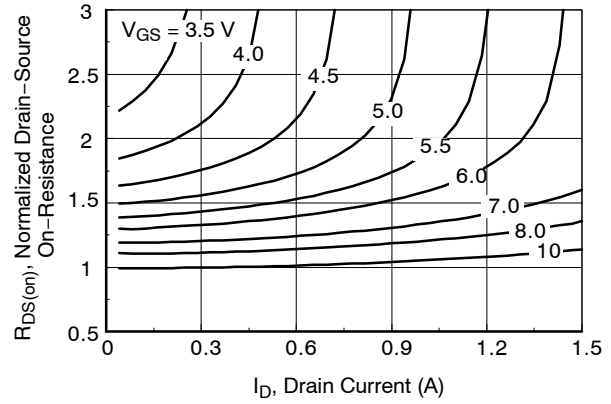


Figure 2. On-Resistance Variation with Gate Voltage and Current

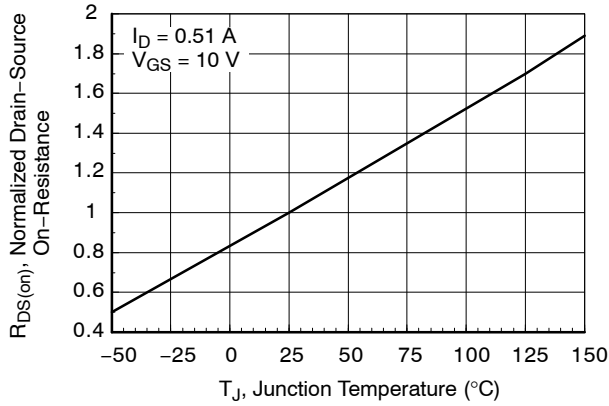


Figure 3. On-Resistance Variation with Temperature

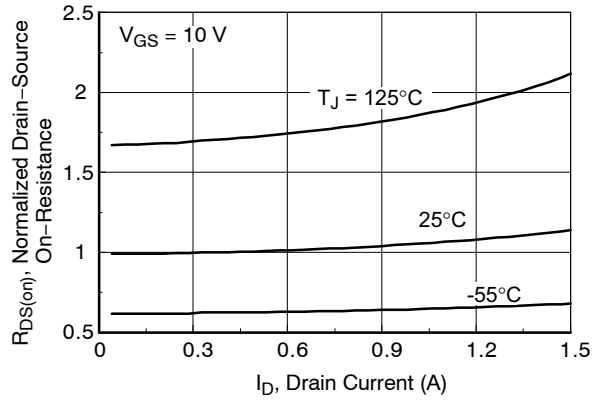


Figure 4. On-Resistance vs Variation with Drain Current and Temperature

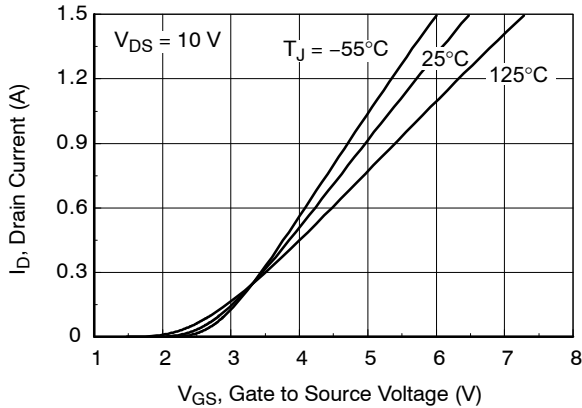


Figure 5. Transfer Characteristics

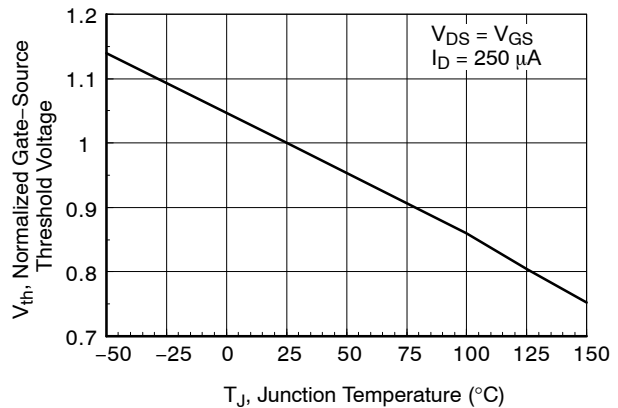


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

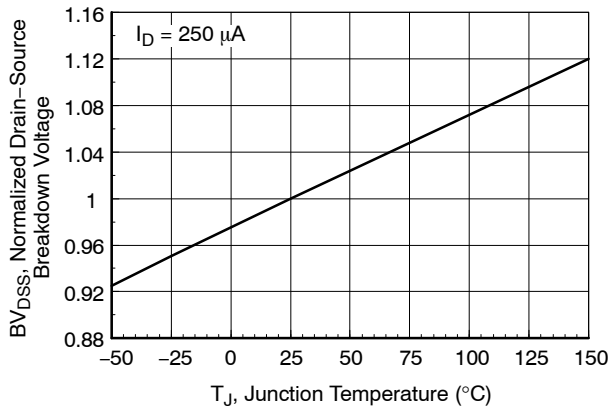


Figure 7. Breakdown Voltage Variation with Temperature

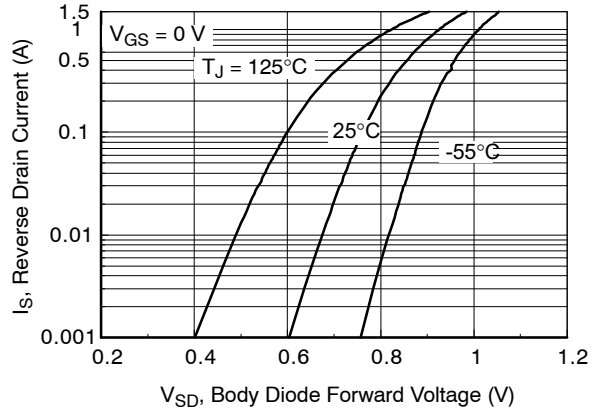


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

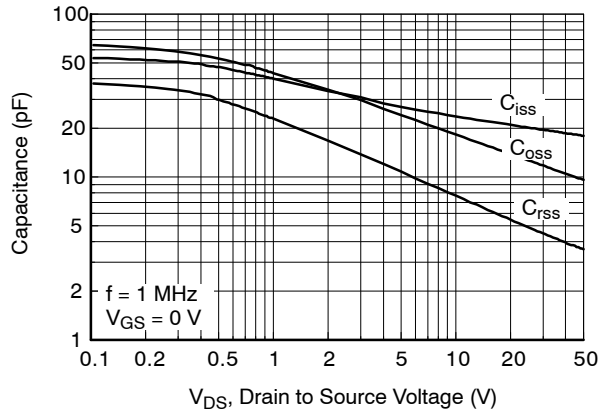


Figure 9. Capacitance Characteristics

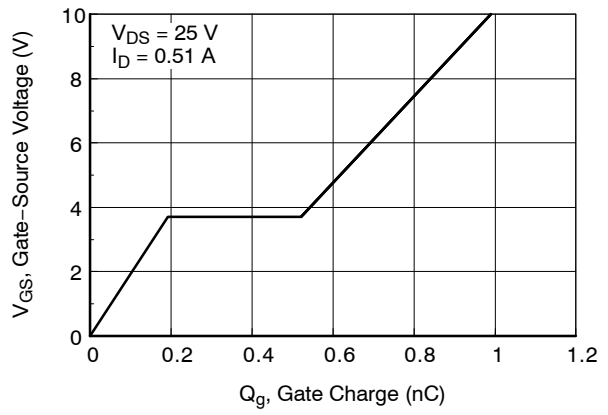


Figure 10. Gate Charge Characteristics

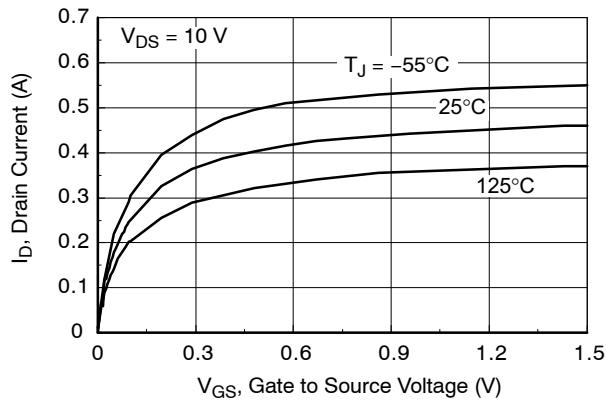


Figure 11. Transconductance Variation with Drain Current and Temperature

TYPICAL THERMAL CHARACTERISTICS

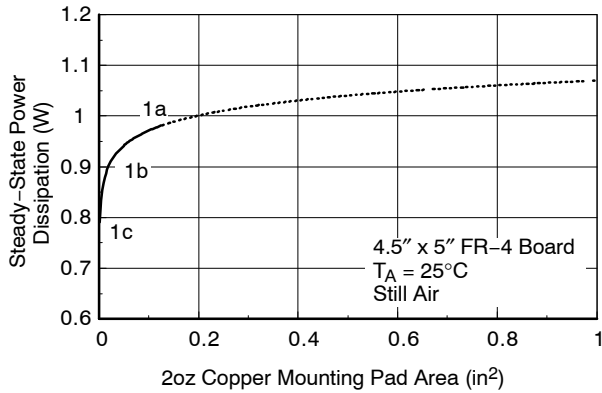


Figure 12. SOT-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area

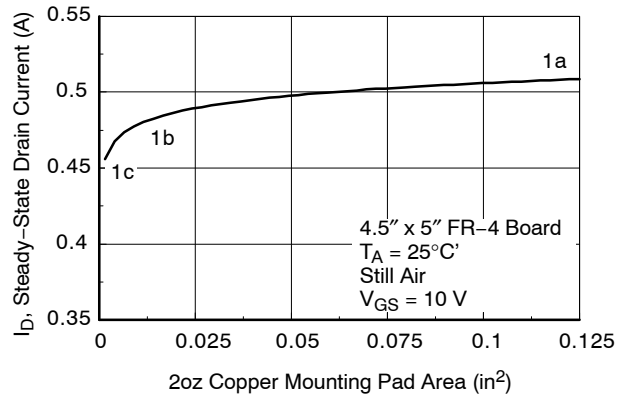


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

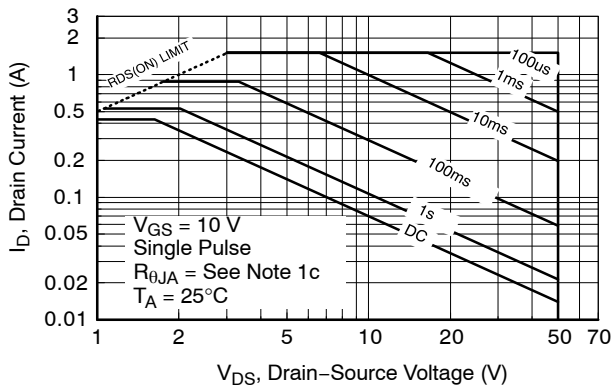


Figure 14. Maximum Safe Operating Area

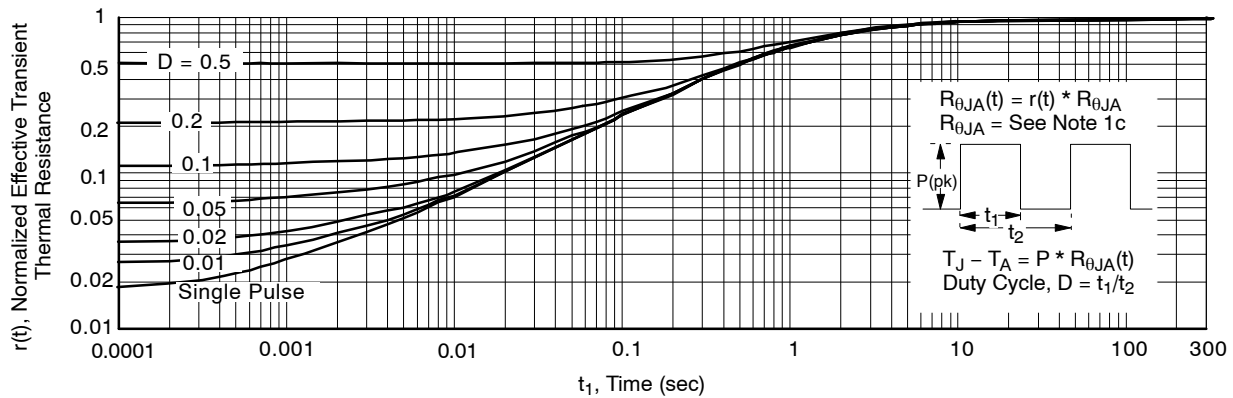


Figure 15. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

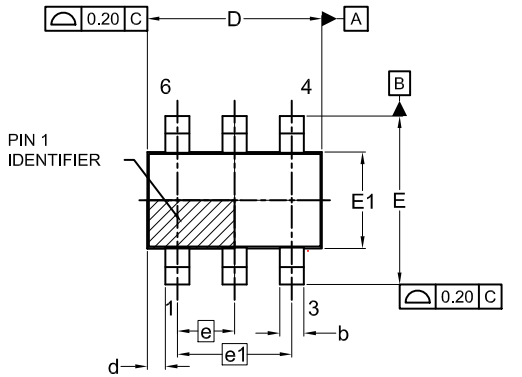
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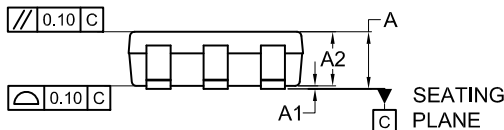
SCALE 2:1

TSOT23 6-Lead CASE 419BL ISSUE A

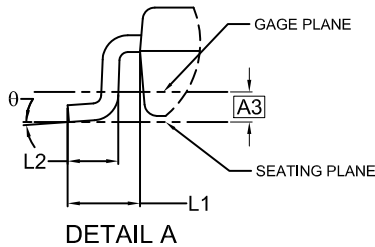
DATE 31 AUG 2020



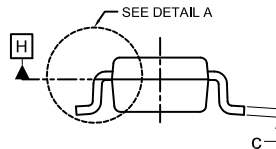
TOP VIEW



FRONT VIEW

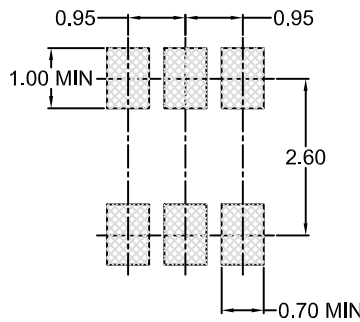


DETAIL A



SIDE VIEW

SYMM
⌀



LAND PATTERN
RECOMMENDATION

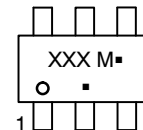
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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