



STD16N65M5, STF16N65M5 STP16N65M5, STU16N65M5

N-channel 650 V, 0.270 Ω , 12 A MDmesh™ V Power MOSFET
DPAK, TO-220FP, TO-220, IPAK

Features

Type	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STD16N65M5	710 V	< 0.299 Ω	12 A
STF16N65M5	710 V	< 0.299 Ω	12 A
STP16N65M5	710 V	< 0.299 Ω	12 A
STU16N65M5	710 V	< 0.299 Ω	12 A

- DPAK worldwide best R_{DS(on)}
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% Avalanche tested

Application

- Switching applications

Description

MDmesh V is a revolutionary Power MOSFET technology, which combines an innovative proprietary vertical process with the well known company's PowerMESH™ horizontal layout. The resulting product has an extremely low on-resistance, unmatched among silicon-based Power MOSFETs, making it especially suited for applications which require superior power density and outstanding efficiencies.

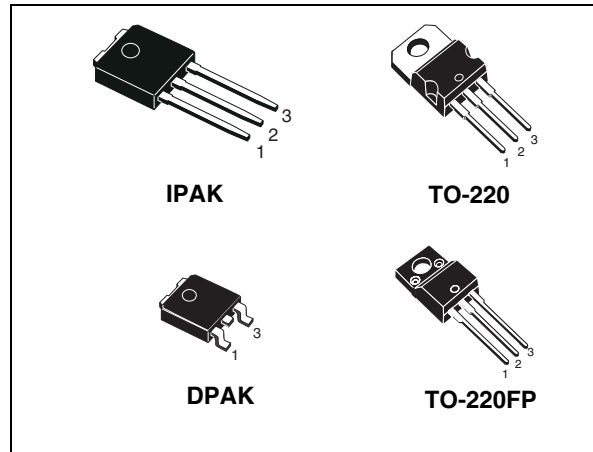


Figure 1. Internal schematic diagram

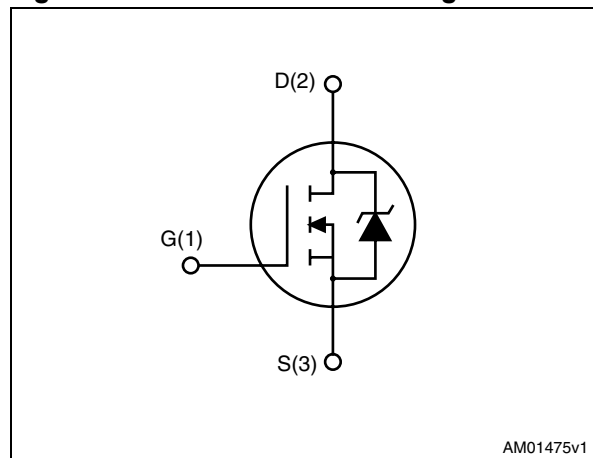


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD16N65M5	16N65M5	DPAK	Tape and reel
STF16N65M5	16N65M5	TO-220FP	Tube
STP16N65M5	16N65M5	TO-220	Tube
STU16N65M5	16N65M5	IPAK	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Packaging mechanical data	15
6	Revision history	16

1 Electrical ratings (a)

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, IPAK, DPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	650		V
V_{GS}	Gate-source voltage	25		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	12	12 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	7.3	7.3 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	48	48 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	90	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)		2500	V
T_{stg}	Storage temperature	- 55 to 50		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	IPAK	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.38		5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		100	62.5		°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50				
T_l	Maximum lead temperature for soldering purpose	300				°C

a. All data which refers solely to the TO-220FP package is preliminary

2 Electrical characteristics^(b)

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		0.270	0.299	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1250		pF
C_{oss}	Output capacitance			30		pF
C_{rss}	Reverse transfer capacitance			3		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$		130		pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			40		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		2		Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)		45		nC
Q_{gs}	Gate-source charge			25		nC
Q_{gd}	Gate-drain charge			10		nC

- $C_{oss\text{ eq}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- $C_{oss\text{ eq}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

b. All data which refers solely to the TO-220FP package is preliminary

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17)		25		ns
t_r	Rise time			9		ns
$t_{d(off)}$	Turn-off-delay time			30		ns
t_f	Fall time			7		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 20)		300		ns
Q_{rr}	Reverse recovery charge			3.5		nC
I_{RRM}	Reverse recovery current			23		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20)		350		ns
Q_{rr}	Reverse recovery charge			4		nC
I_{RRM}	Reverse recovery current			24		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK, IPAK, TO-220

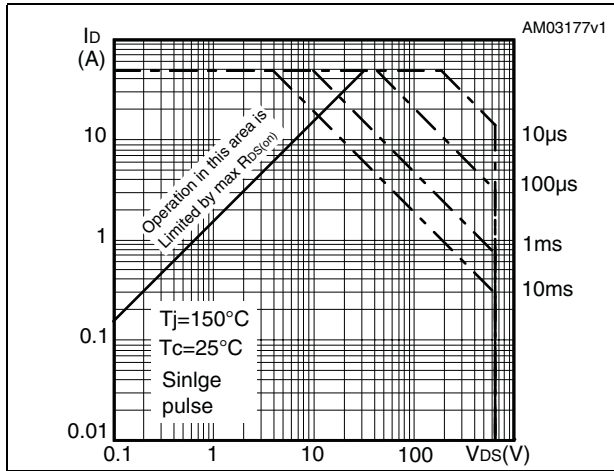


Figure 3. Thermal impedance for DPAK, IPAK, TO-220

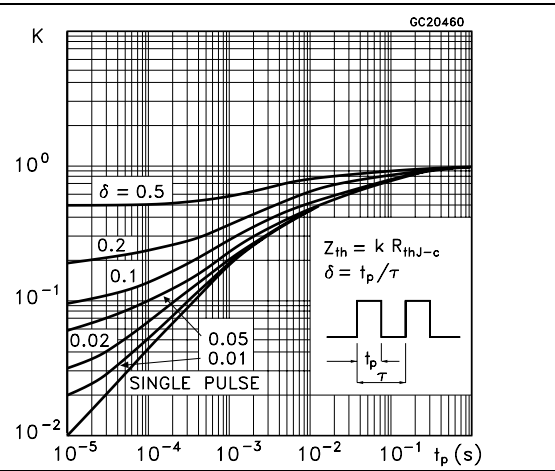


Figure 4. Output characteristics

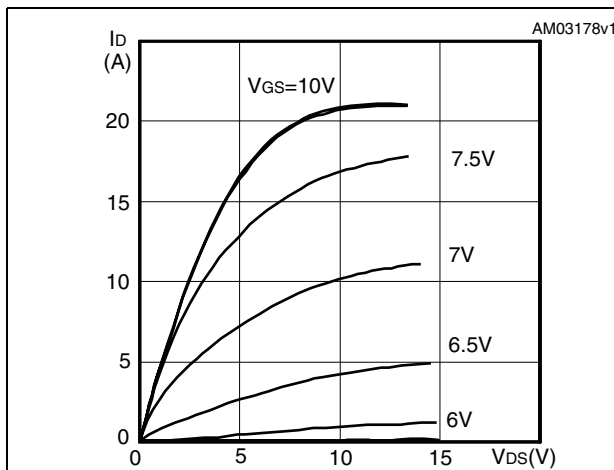


Figure 5. Transfer characteristics

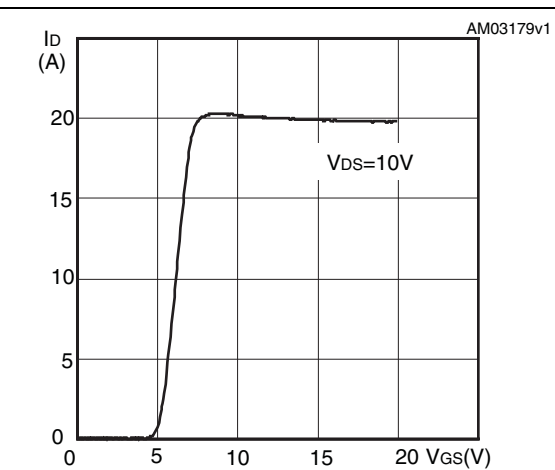


Figure 6. Transconductance

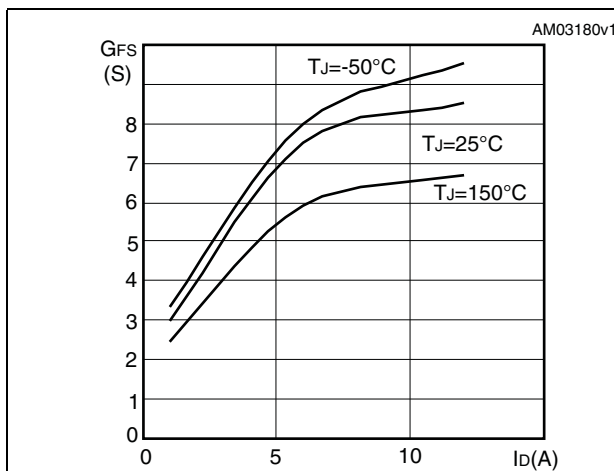


Figure 7. Static drain-source on resistance

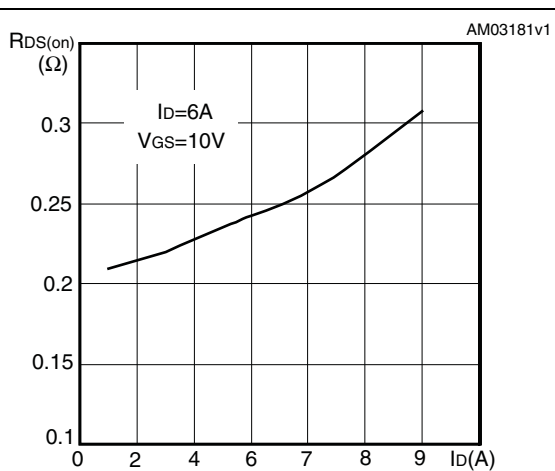


Figure 8. Output capacitance stored energy Figure 9. Capacitance variations

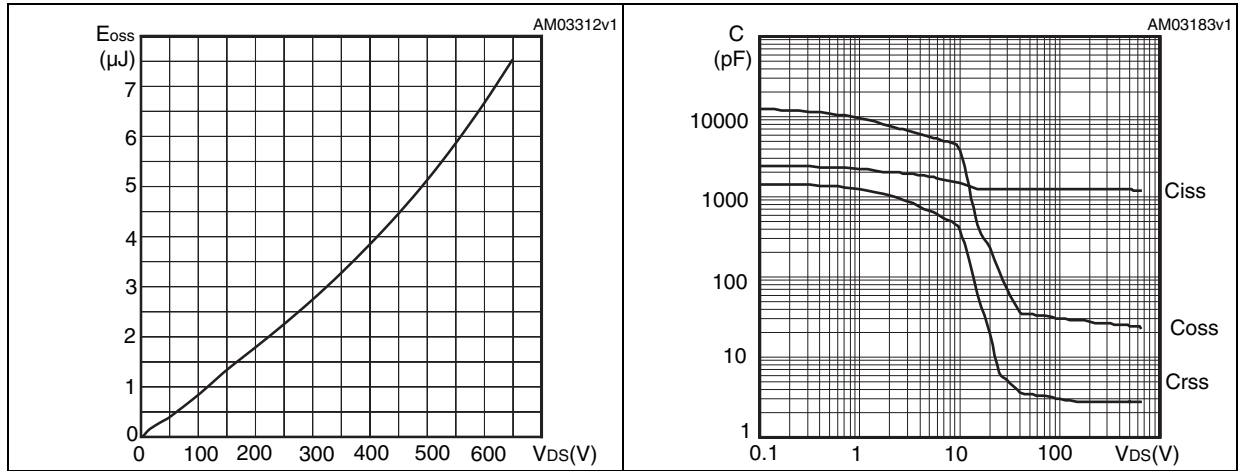


Figure 10. Gate charge vs gate-source voltage Figure 11. Normalized on resistance vs temperature

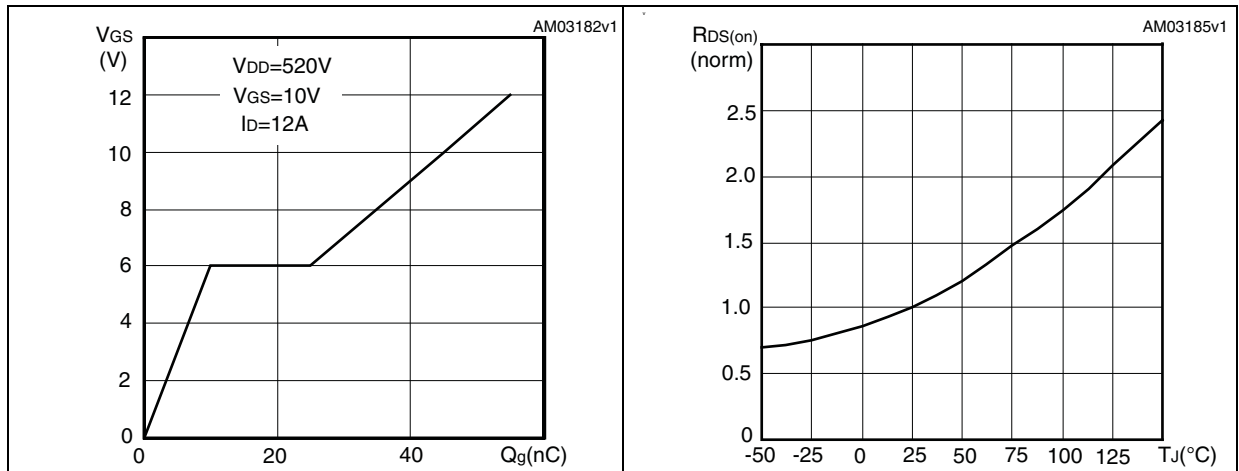


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized $B_{V_{DS}}$ vs temperature

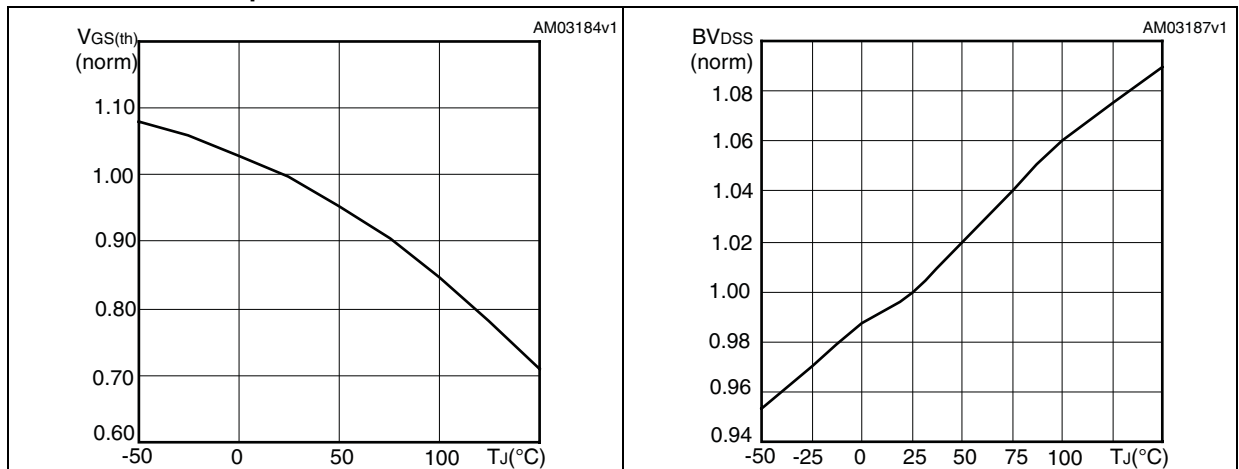
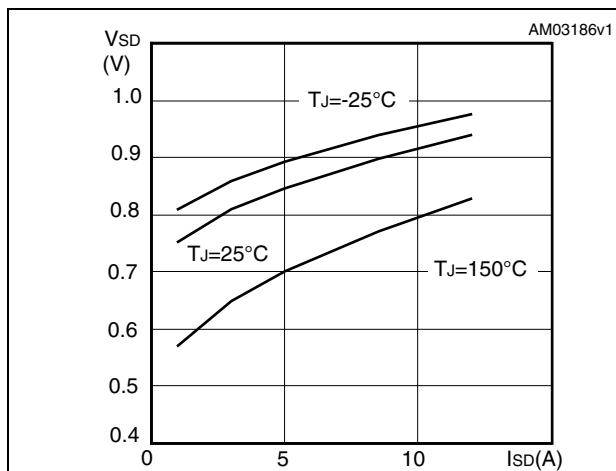


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

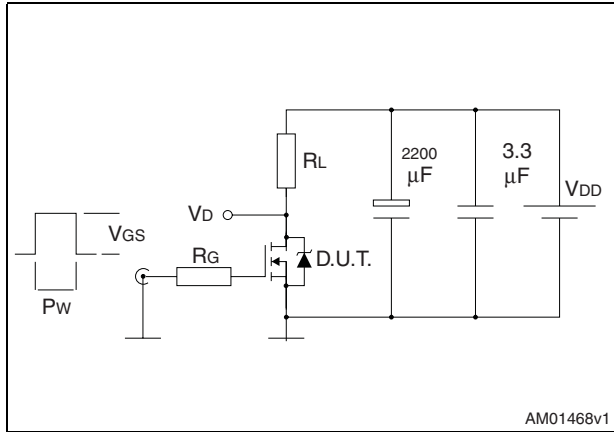


Figure 16. Gate charge test circuit

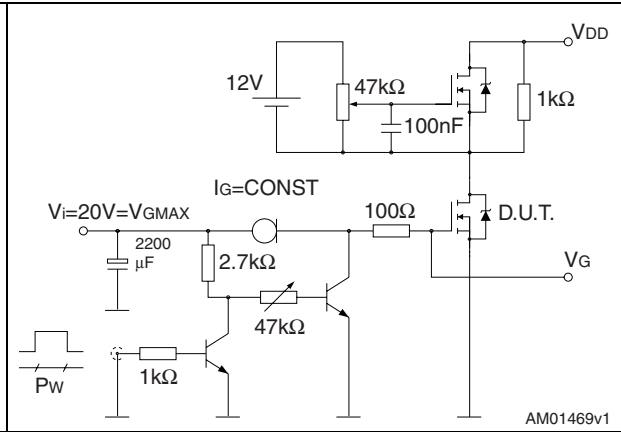


Figure 17. Test circuit for inductive load switching and diode recovery times

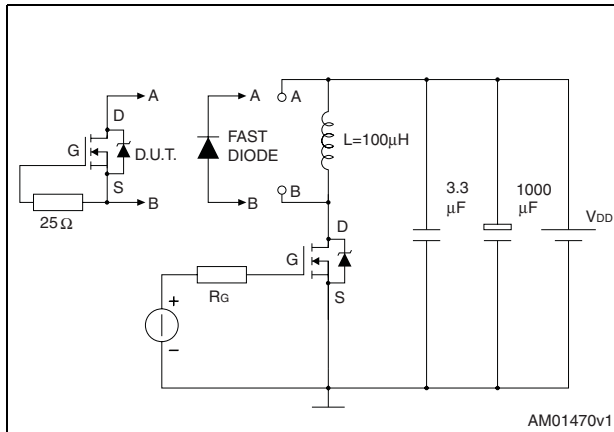


Figure 18. Unclamped inductive load test circuit

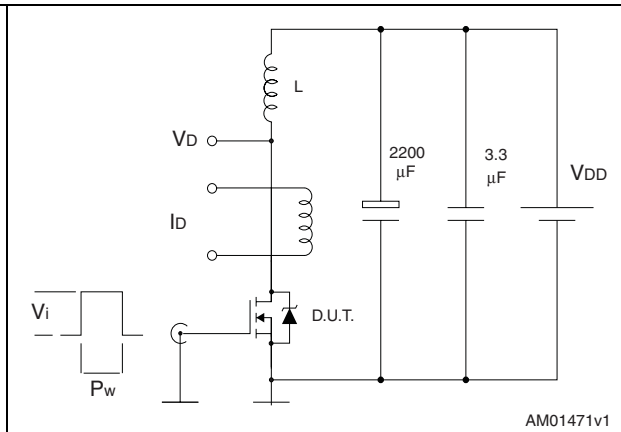


Figure 19. Unclamped inductive waveform

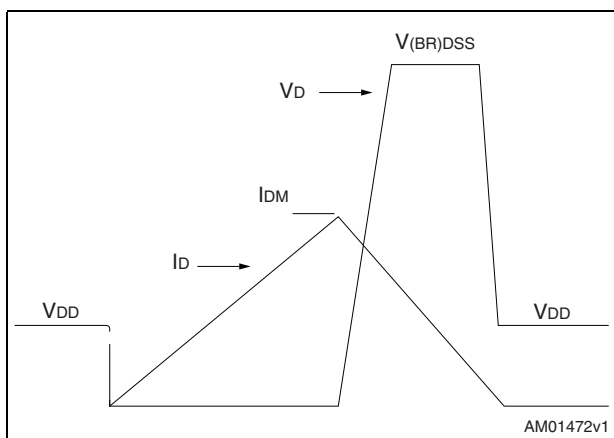
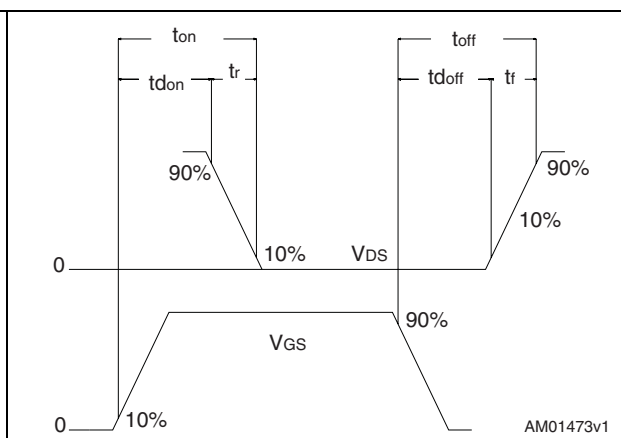


Figure 20. Switching time waveform

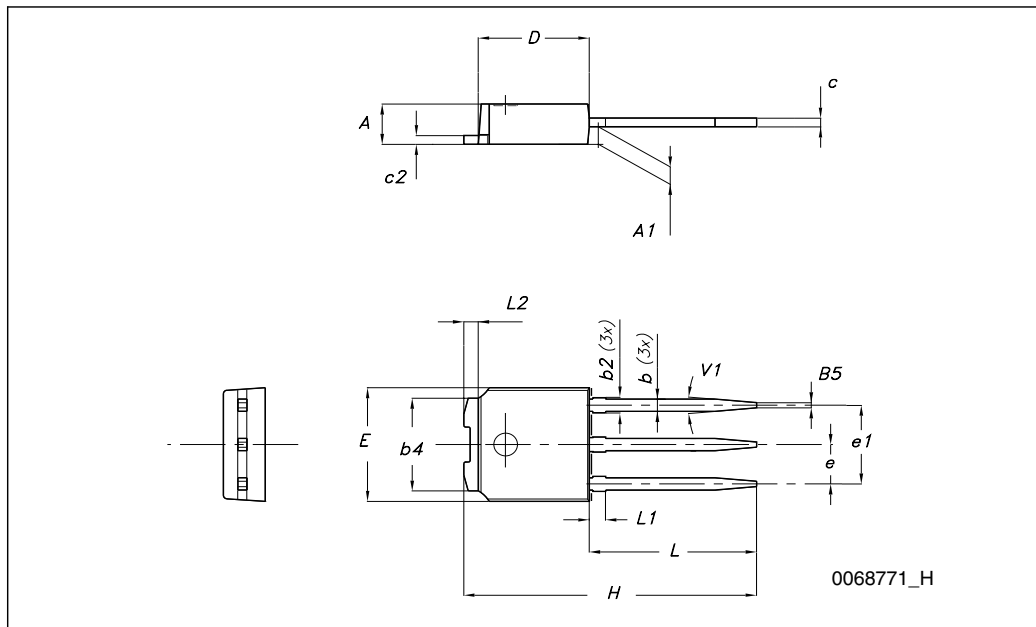


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

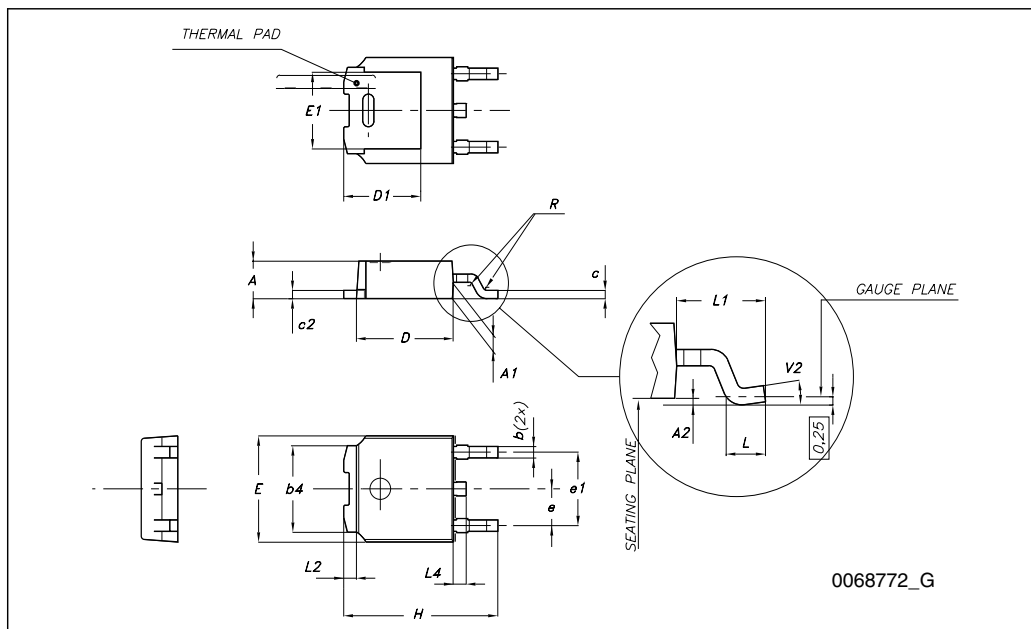
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



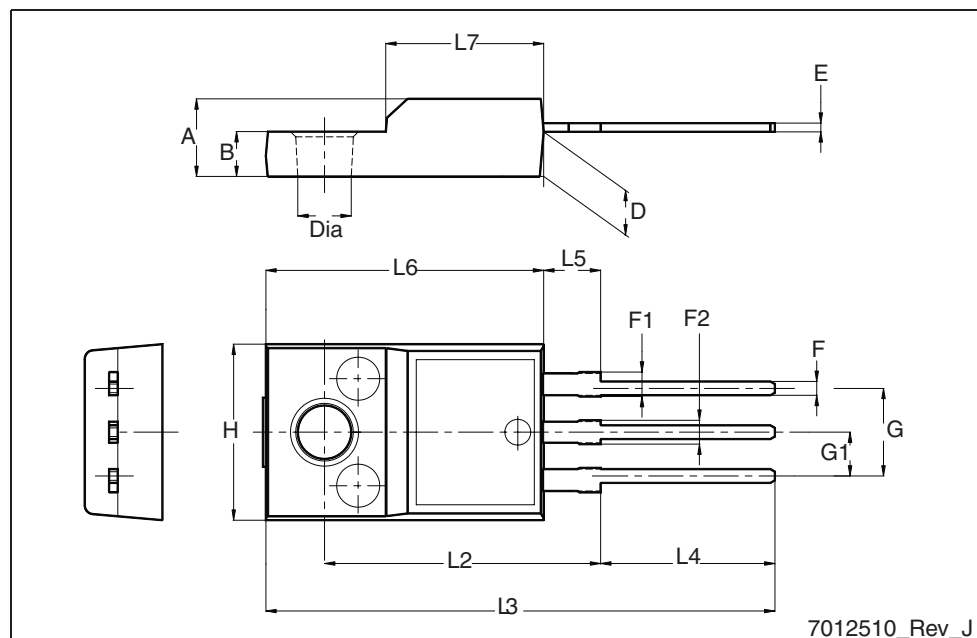
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



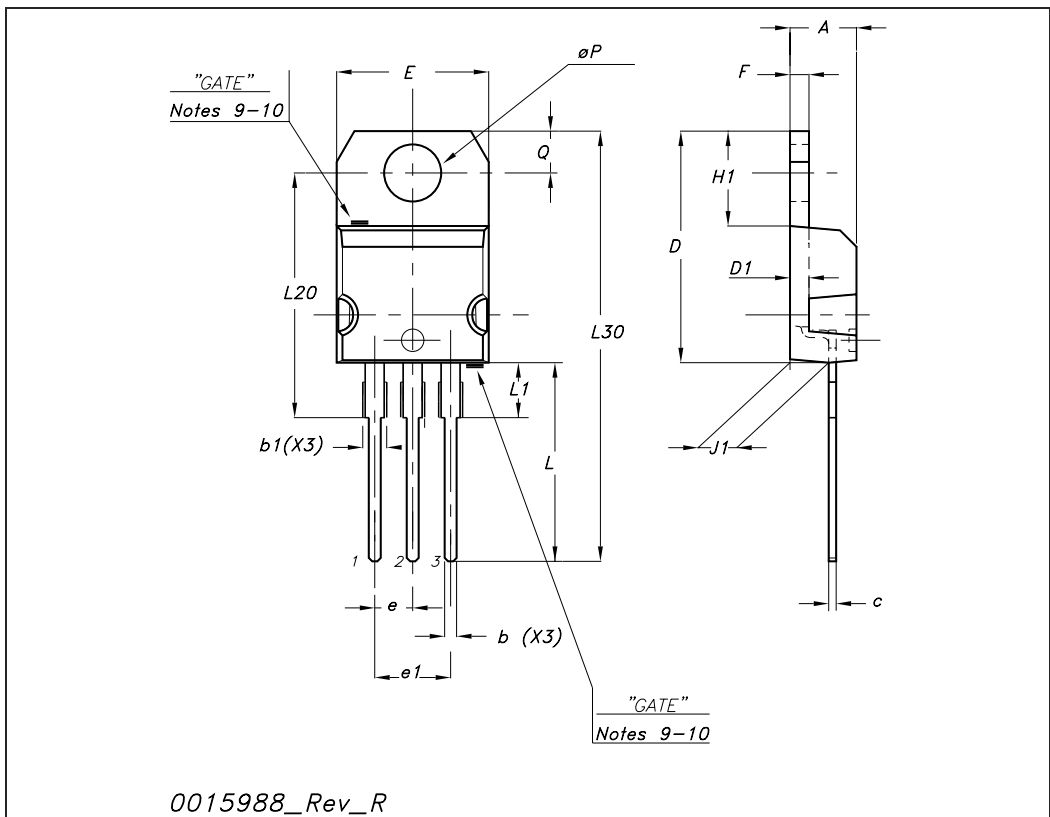
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



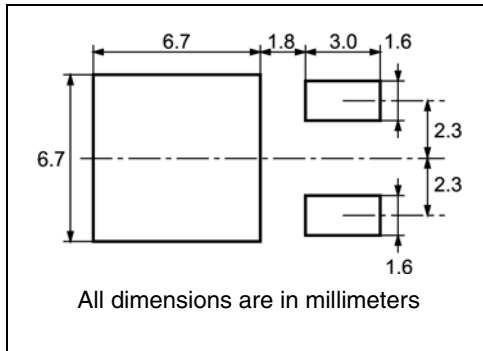
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-Feb-2009	1	First release

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