PD - 95466

International
IOR Rectifier

AUTOMOTIVE MOSFET

IRF3710ZPbF
IRF3710ZSPbF
IRF3710ZLPbF

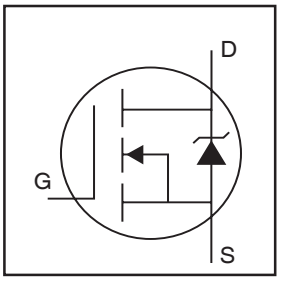
HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



V_{DSS} = 100V

$R_{DS(on)}$ = 18mΩ

I_D = 59A

TO-220AB IRF3710Z | D^2Pak IRF3710ZS | TO-262 IRF3710ZL

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	59	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (See Fig. 9)	42	
I_{DM}	Pulsed Drain Current ①	240	
P_D @T_C = 25°C	Maximum Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	170	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑦	200	
I_{AR}	Avalanche Current ①	See Fig.12a,12b,15,16	A
E_{AR}	Repetitive Avalanche Energy ⑥		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.92	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)⑧	—	40	

HEXFET® is a registered trademark of International Rectifier.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	14	18	mΩ	V_{GS} = 10V, I_D = 35A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Transconductance	35	—	—	S	V_{DS} = 50V, I_D = 35A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	82	120	nC	I_D = 35A
Q_{gs}	Gate-to-Source Charge	—	19	28		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	27	40		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 50V
t_r	Rise Time	—	77	—		I_D = 35A
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		R_G = 6.8Ω
t_f	Fall Time	—	56	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package and center of die contact
C_{iss}	Input Capacitance	—	2900	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	290	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	1130	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	170	—		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	280	—		V_{GS} = 0V, V_{DS} = 0V to 80V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	59	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	240		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 35A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	50	75	ns	T_J = 25°C, I_F = 35A, V_{DD} = 25V
Q_{rr}	Reverse Recovery Charge	—	100	160	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.27mH, R_G = 25Ω, I_{AS} = 35A, V_{GS} =10V. Part not recommended for use above this value.

③ I_{SD} ≤ 35A, di/dt ≤ 380A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑦ This value determined from sample failure population. 100% tested to this value in production.

⑧ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

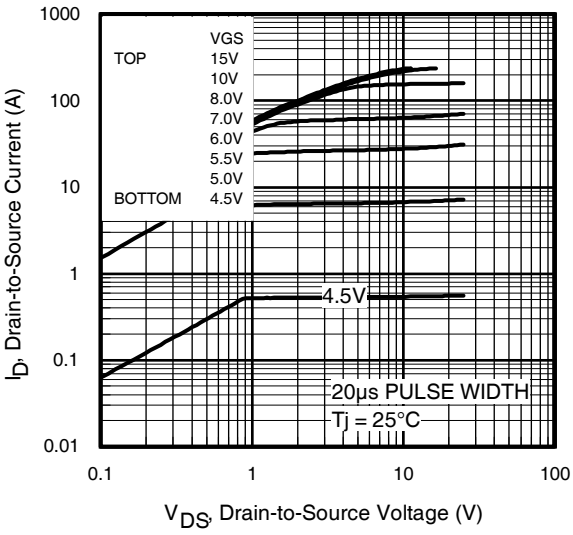


Fig 1. Typical Output Characteristics

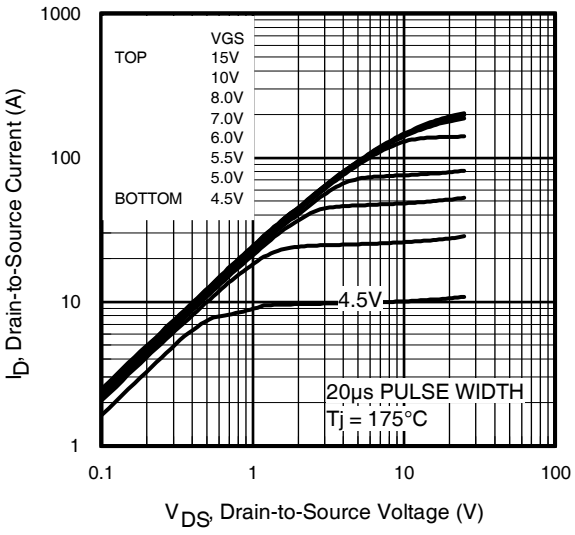


Fig 2. Typical Output Characteristics

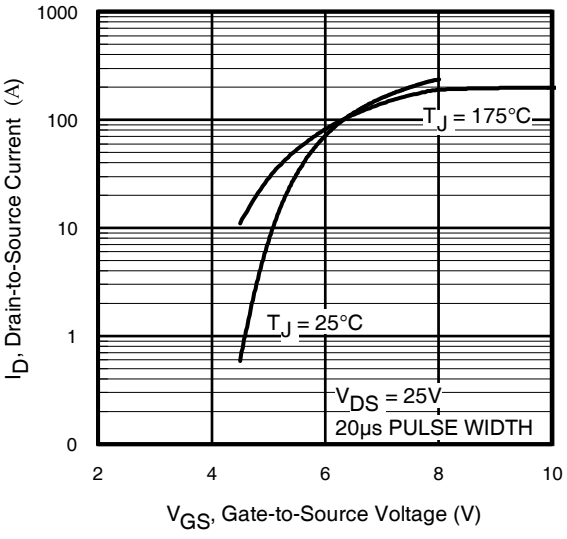


Fig 3. Typical Transfer Characteristics

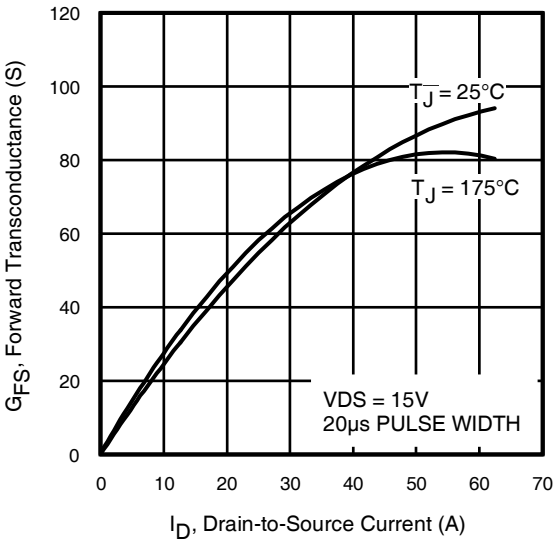


Fig 4. Typical Forward Transconductance vs. Drain Current

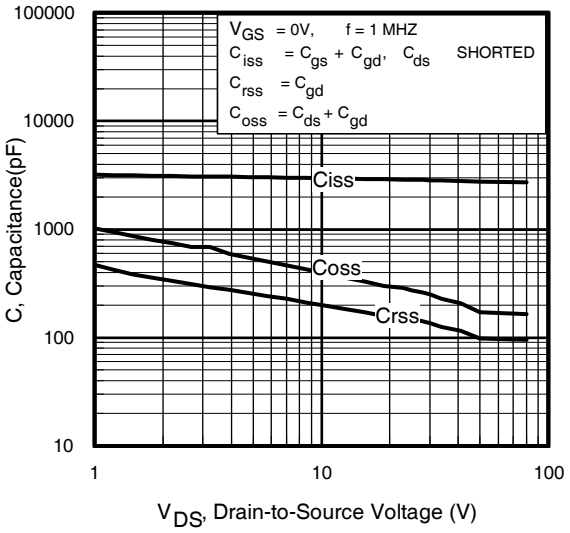


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

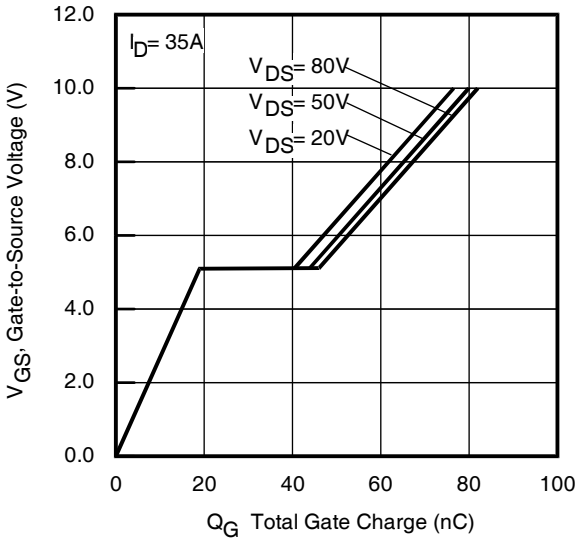


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

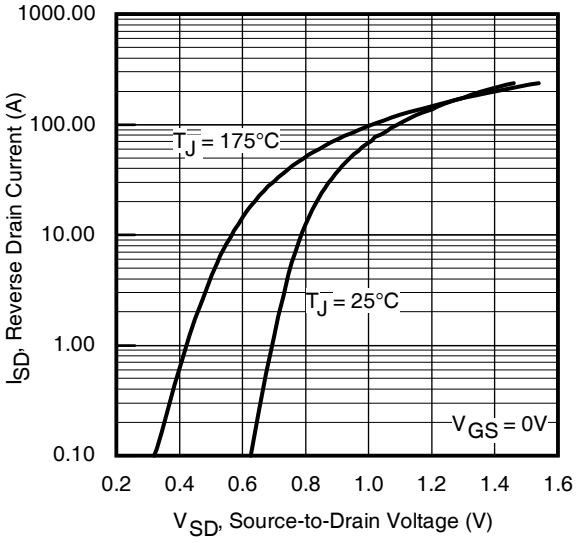


Fig 7. Typical Source-Drain Diode Forward Voltage

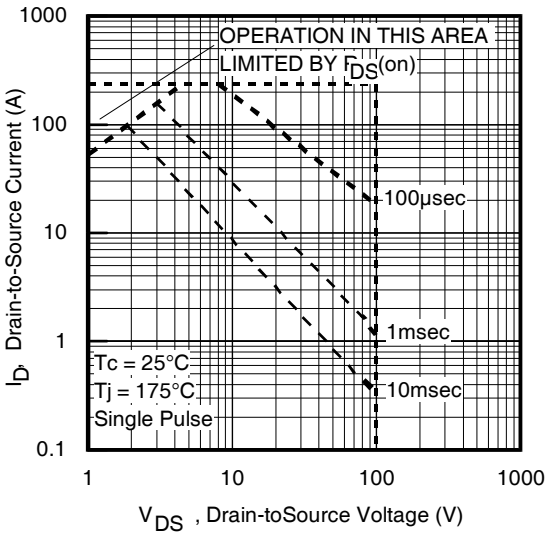


Fig 8. Maximum Safe Operating Area

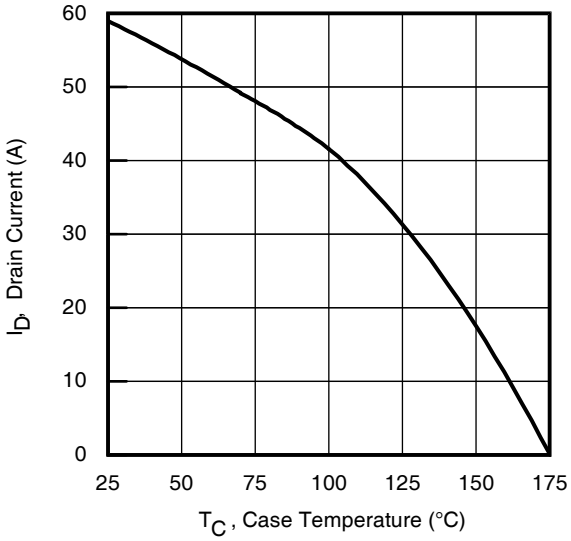


Fig 9. Maximum Drain Current vs. Case Temperature

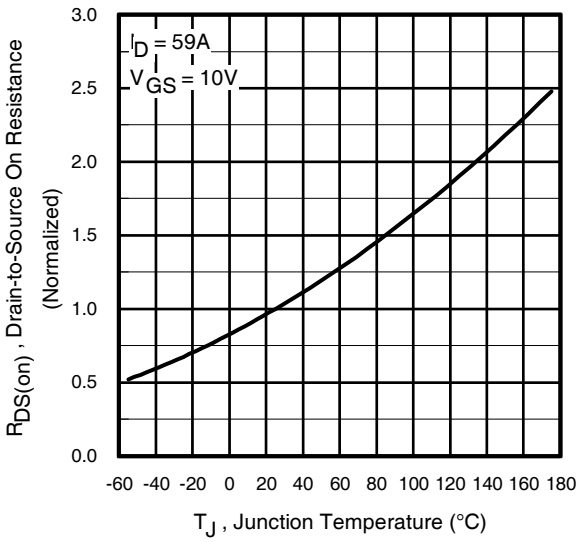


Fig 10. Normalized On-Resistance vs. Temperature

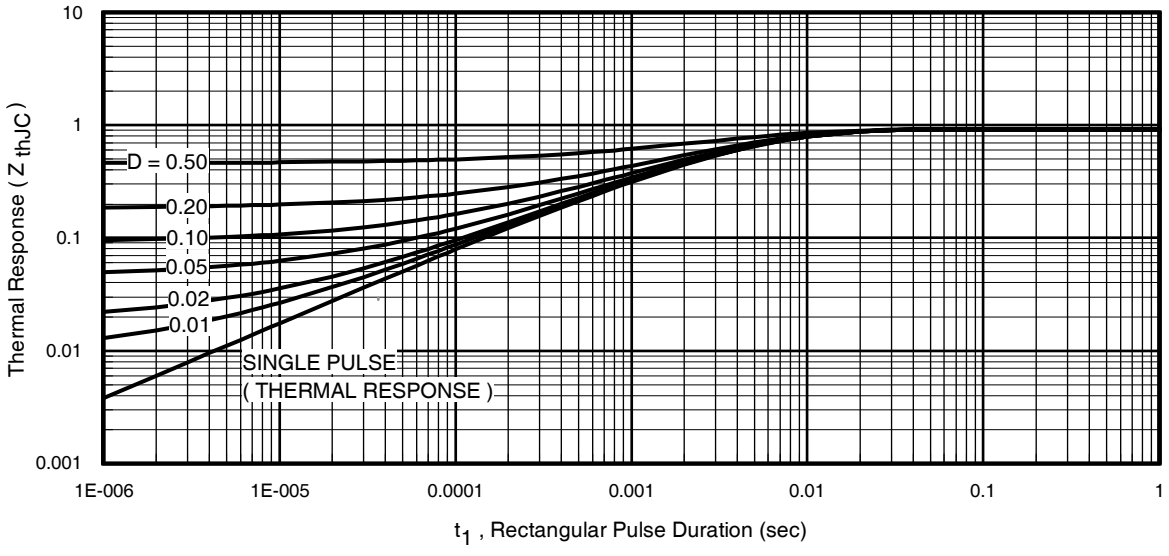


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

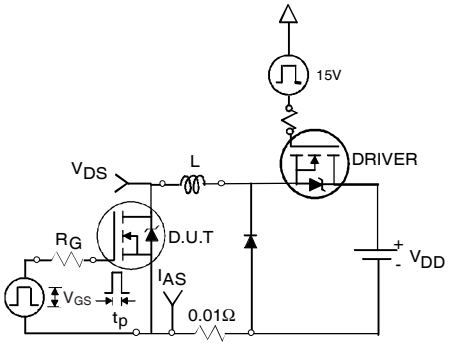


Fig 12a. Unclamped Inductive Test Circuit

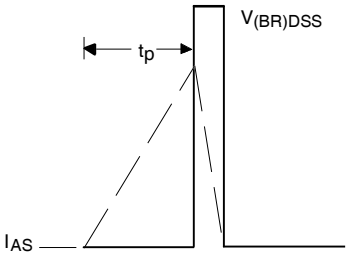


Fig 12b. Unclamped Inductive Waveforms

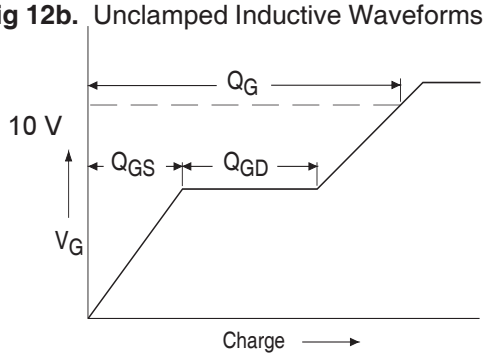


Fig 13a. Basic Gate Charge Waveform

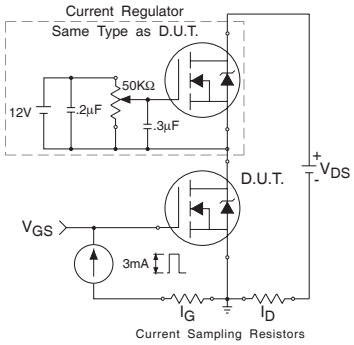


Fig 13b. Gate Charge Test Circuit

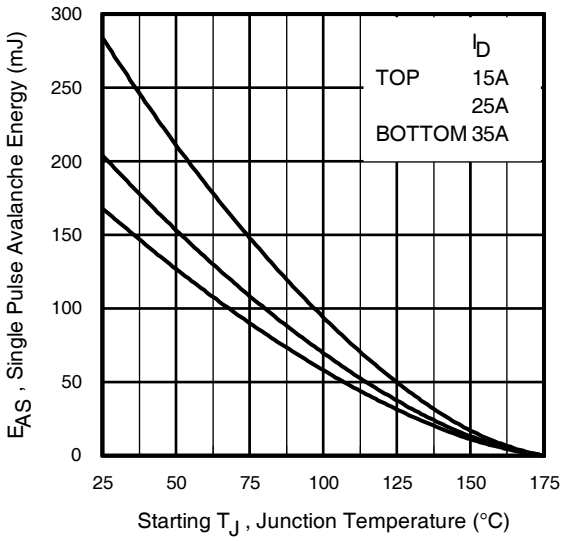


Fig 12c. Maximum Avalanche Energy vs. Drain Current

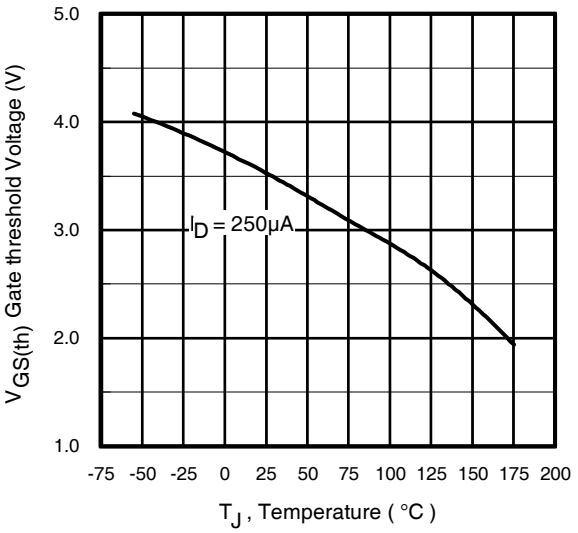


Fig 14. Threshold Voltage vs. Temperature

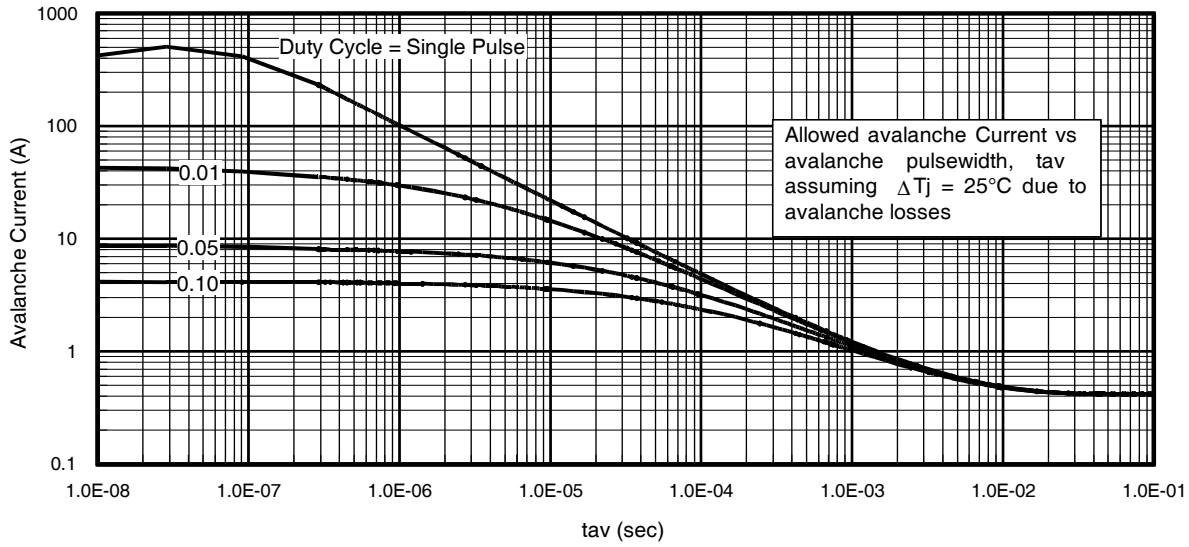


Fig 15. Typical Avalanche Current vs.Pulsewidth

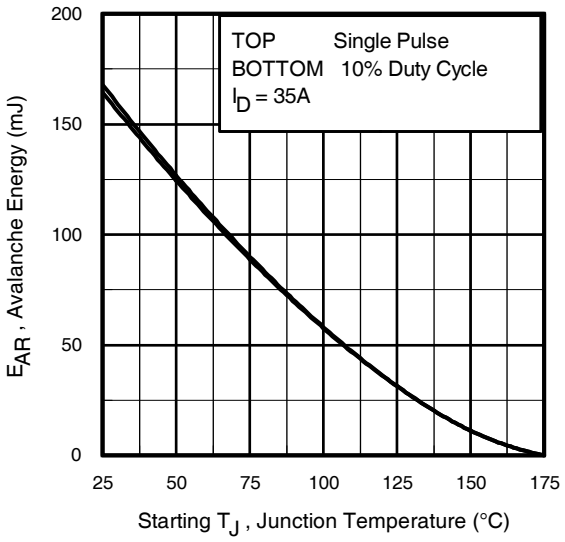


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

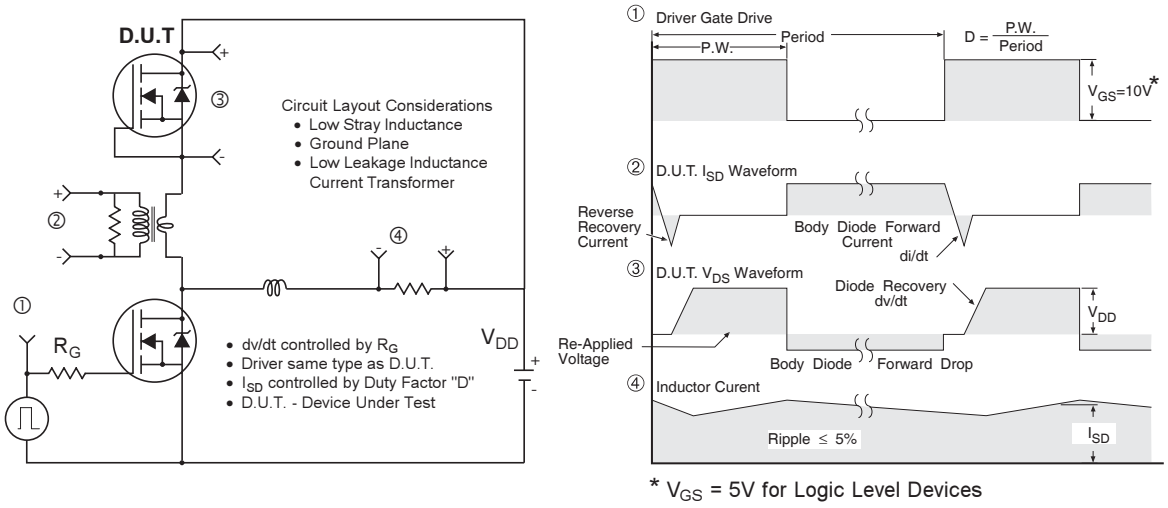


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

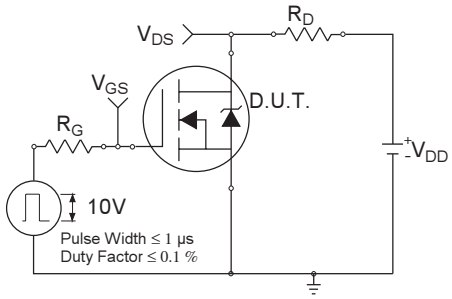


Fig 18a. Switching Time Test Circuit

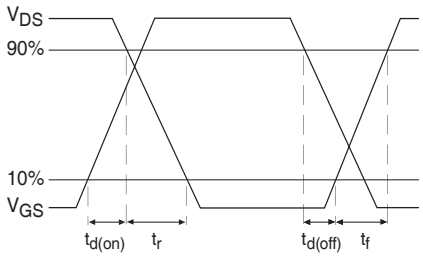
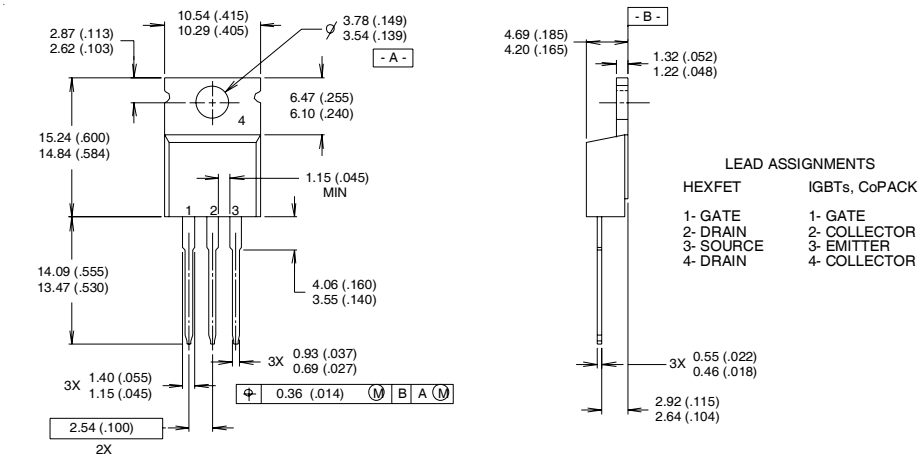


Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



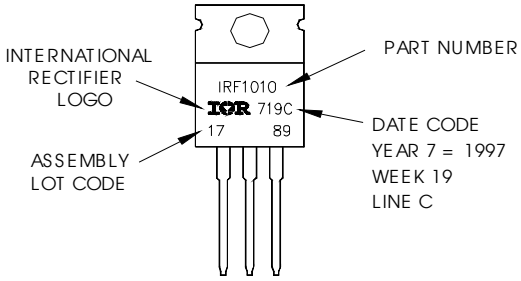
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

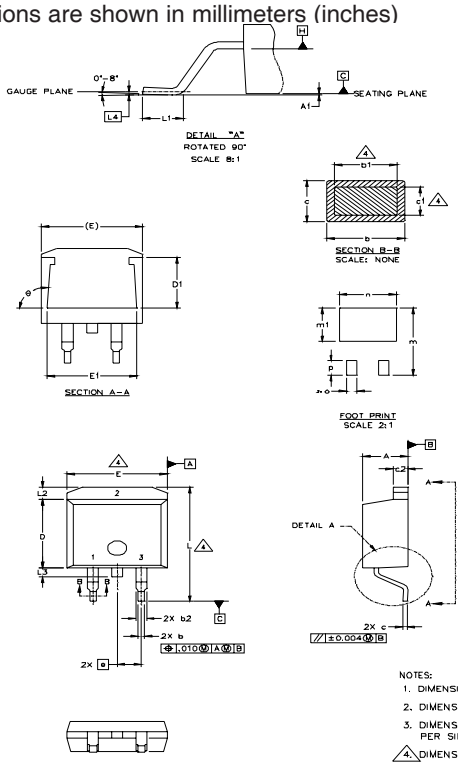
EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.– GATE	1.– GATE	1.– ANODE *
2.– DRAIN	2.– COLLECTOR	2.– CATHODE
3.– SOURCE	3.– EMITTER	3.– ANODE

* PART DEPENDENT.

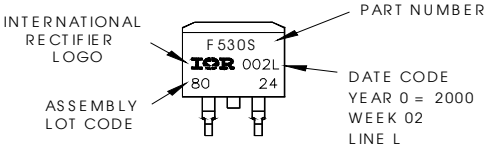
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

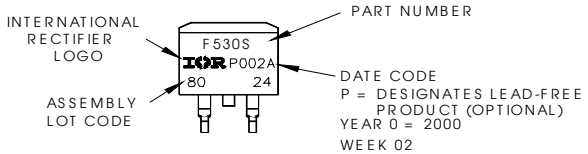
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

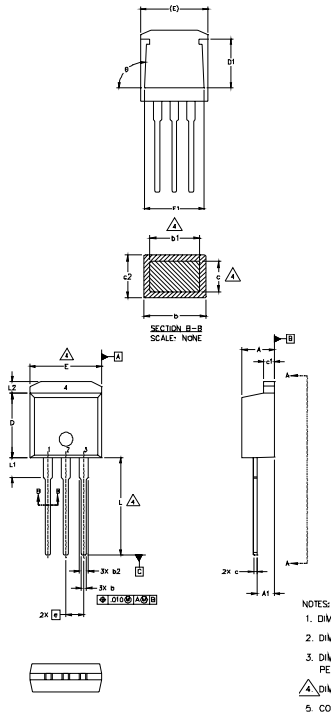
Note: "P" in assembly line
position indicates "Lead-Free"



OR



TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

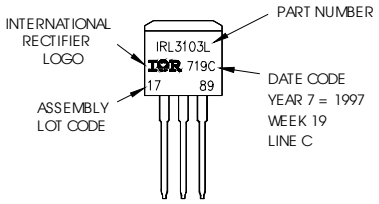
HEXFET	IGBT
1.– GATE	1- GATE
2.– DRAIN	2- COLLECTOR
3.– SOURCE	3- EMITTER
4.– DRAIN	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

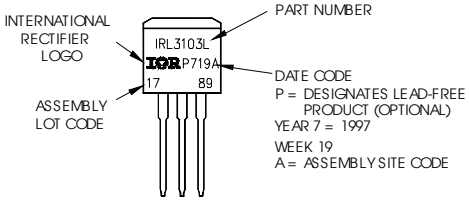
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

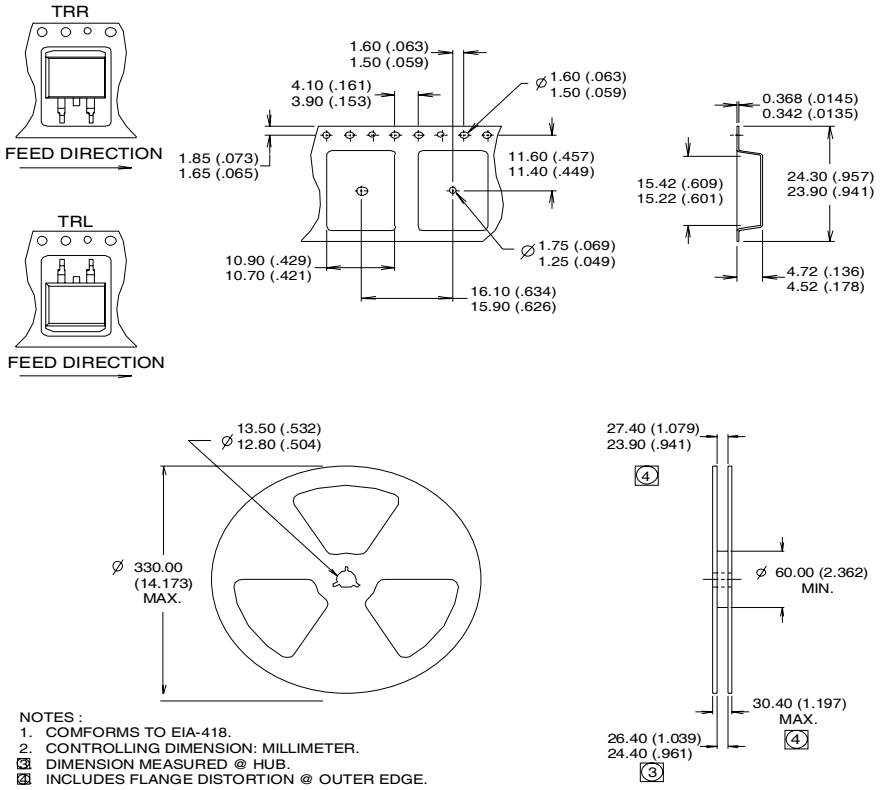


OR



D^{2}Pak Tape & Reel Infomation

Dimensions are shown in millimeters (inches)



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/