OPAx130 Low-Power, Precision FET-Input Operational Amplifiers

1 Features

- Low quiescent current: 530µA/amp
- Low offset voltage: 1mV max
- High open-loop gain: 123dB (R_L = 10kΩ)
- High CMRR: 90dB min
- FET input: I_B = 20pA max
- Excellent bandwidth: 1MHz
- Wide supply range: ±2.25V to ±18V
- Single, dual, and quad versions

2 Applications

- Data acquisition (DAQ)
- Flow transmitter
- Lab and field instrumentation
- Electrocardiogram (ECG)

3 Description

The OPA130, OPA2130, and OPA4130 (OPAx130) series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. OPAx130 are designed for general-purpose, portable, and battery operated applications, especially with high source impedance.

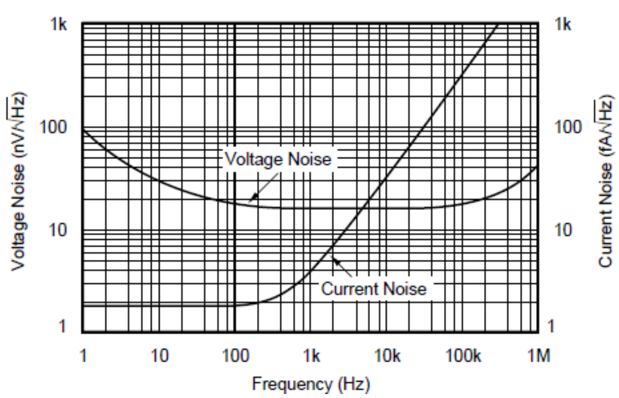
OPAx130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over the wide input voltage range of the amplifier. OPAx130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in an 8-pin SOIC surface-mount package. The quad version is available in a 14-pin SOIC surface-mount package. All devices are specified for –40°C to +85°C operation.

Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA130	Single	D (SOIC, 8)
OPA2130	Dual	D (SOIC, 8)
OPA4130	Quad	D (SOIC, 14)

(1) For more information, see Section 9.



Input Voltage and Current Noise Spectral Density vs Frequency

Table of Contents

4 Pin Configuration and Functions

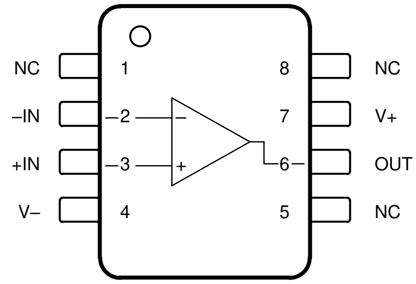


Figure 4-1. OPA130 D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: OPA130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input, channel A
–IN	2	Input	Inverting input, channel A
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

(1) Existing layouts for the OPA130 D package before revision B of this data sheet do not need to be redesigned.

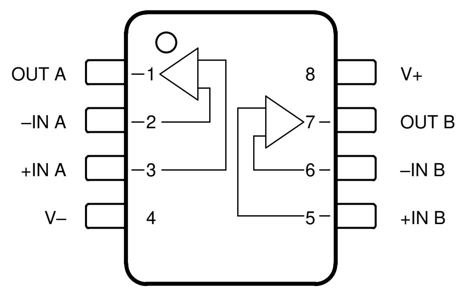


Figure 4-2. OPA2130 D Package, 8-Pin SOIC (Top View)

Table 4-2. Pin Functions: OPA2130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

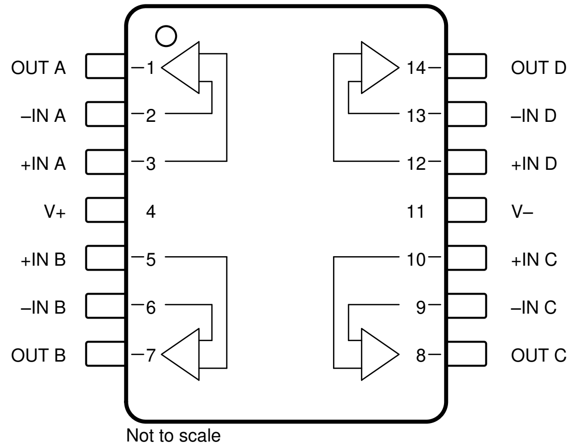


Figure 4-3. OPA4130 D Package, 14-Pin SOIC (Top View)

Table 4-3. Pin Functions: OPA4130

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	11	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±18	V
		Single supply		36	
	Input voltage[(2)]		(V–) – 0.5	(V+) + 0.5	V
	Input current[(2)]			±10	mA
I_{SC}	Output short-circuit[(3)]		Continuous		
T_A	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±2.25	±15	±18	V
		Single supply	4.5	30	36	
T_A	Ambient temperature		–40	25	85	°C

5.3 Thermal Information - OPA130

THERMAL METRIC[(1)]		OPA130 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information - OPA2130

THERMAL METRIC[(1)]		OPA2130 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA4130

THERMAL METRIC[(1)]		OPA4130 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2	±10	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±2.25V to ±18V			±2	±20	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±20	pA
		T_A = –40°C to +85°C		See *Typical Characteristics*			pA
I_{OS}	Input offset current(1)				±2	±20	pA
NOISE							
e_n	Input voltage noise density	f = 10Hz			30		nV/√Hz
		f = 100Hz			18		
		f = 1kHz			16		
		f = 10kHz			16		
I_n	Input current noise density	f = 1kHz			4		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) + 2		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	–13V ≤ V_{CM} ≤ 11.5V		90	105		dB
INPUT IMPEDANCE							
	Differential				10^{13} || 5		Ω || pF
	Common-mode	–13V ≤ V_{CM} ≤ 11.5V			10^{13} || 4.3		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–13.8V ≤ V_O ≤ 13V, R_L = 10kΩ		114	123		dB
		–13V ≤ V_O ≤ 12V, R_L = 2kΩ		104	110		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1		MHz
SR	Slew rate				2		V/μs
	Settling time	10V step, G = 1	0.1%		5.5		μs
			0.01%		7		
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3.5V_{rms}			0.0003%		
	Overload recovery time	G = 1, V_{IN} = ±15V			2		μs
OUTPUT							
V_O	Voltage output	R_L = 10kΩ	Positive	(V+) – 2	(V+) – 1.5		V
			Negative		(V–) + 1	(V–) + 1.2	
		R_L = 2kΩ	Positive	(V+) – 3	(V+) – 2.5		
			Negative		(V–) + 1.5	(V–) + 2	
I_{SC}	Short-circuit current				±18		mA
C_{LOAD}	Capacitive load drive	Stable operation		See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0mA			±530	±650	μA

(1) High-speed test at T_J = 25°C.

5.7 Typical Characteristics

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)

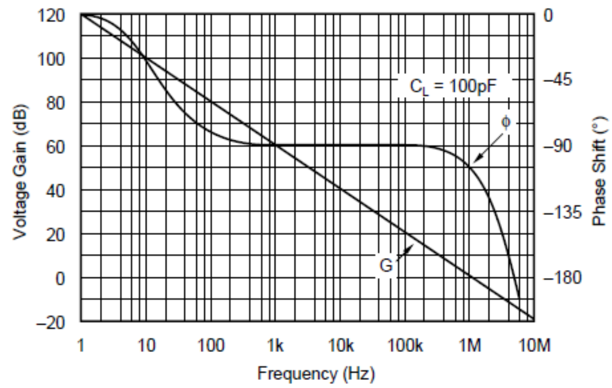


Figure 5-1. Open-Loop Gain and Phase vs Frequency

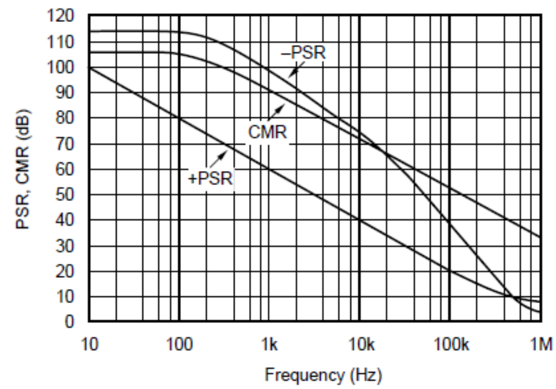


Figure 5-2. Power Supply and Common-Mode Rejection vs Frequency

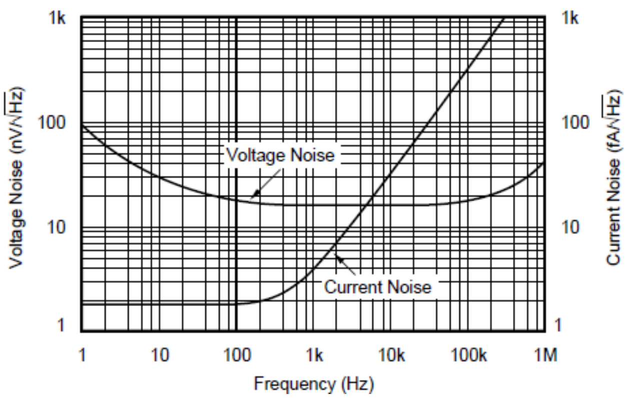


Figure 5-3. Input Voltage and Current Noise Spectral Density vs Frequency

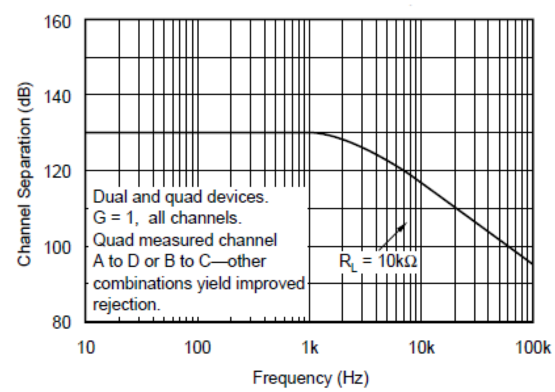


Figure 5-4. Channel Separation vs Frequency

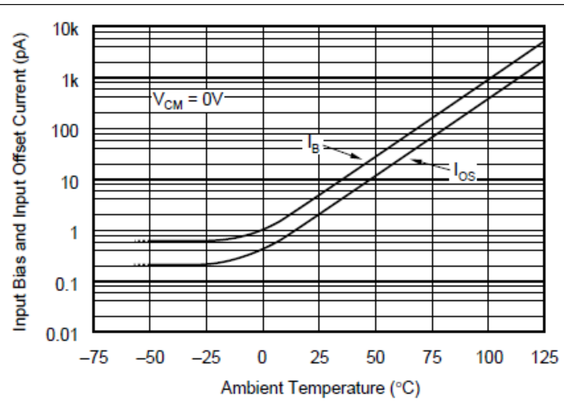


Figure 5-5. Input Bias and Input Offset Current vs Temperature

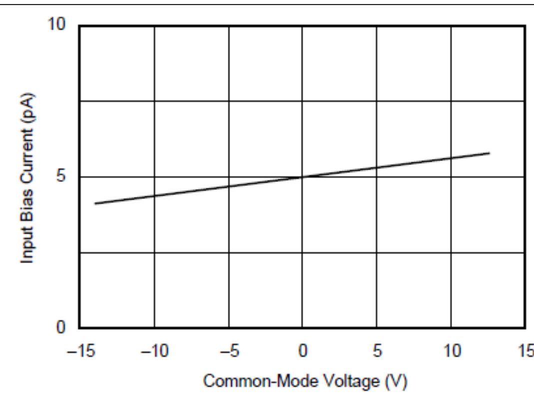


Figure 5-6. Input Bias Current vs Input Common-Mode Voltage

5.7 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)

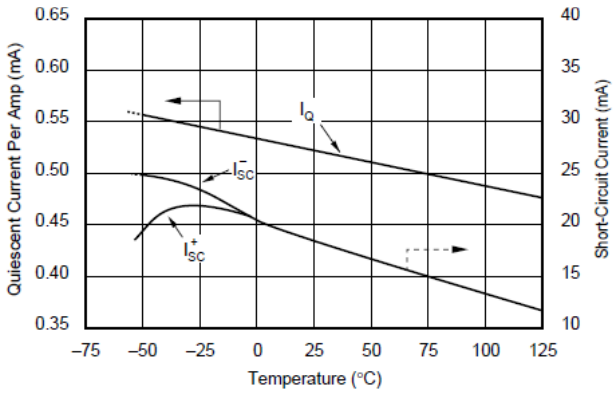


Figure 5-7. Quiescent Current and Short-Circuit Current vs Temperature

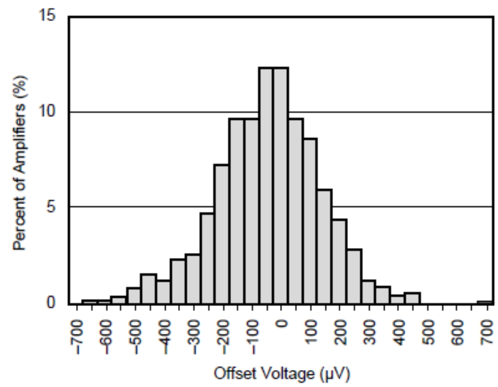


Figure 5-8. Offset Voltage Production Distribution

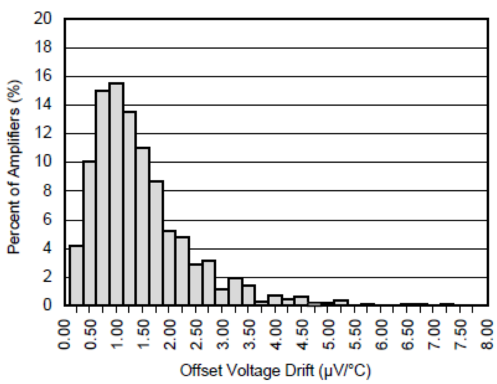


Figure 5-9. Offset Voltage Drift Production Distribution

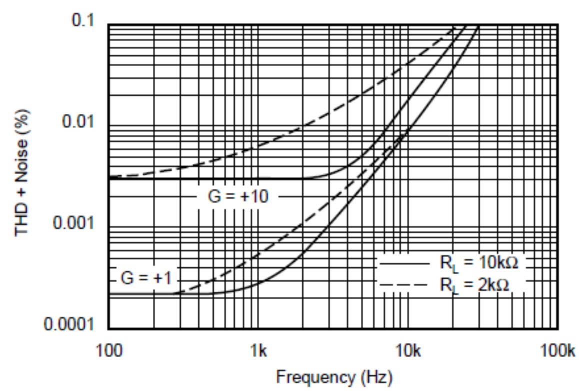


Figure 5-10. Total Harmonic Distortion + Noise vs Frequency

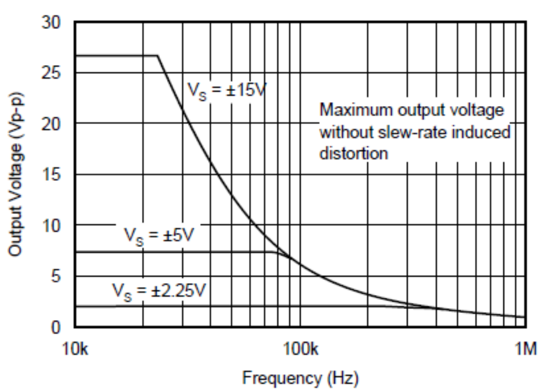
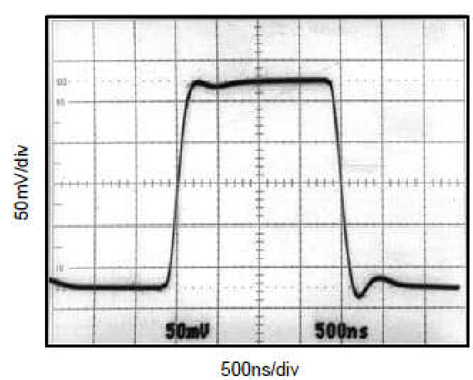


Figure 5-11. Maximum Output Voltage vs Frequency

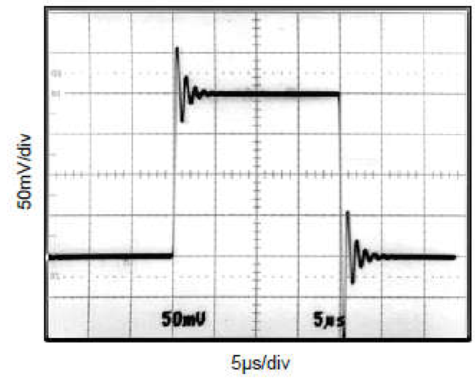


G = 1, C_L = 100pF

Figure 5-12. Small-Signal Step Response

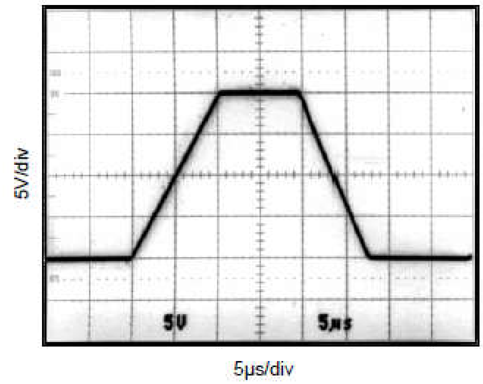
5.7 Typical Characteristics (continued)

at T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = midsupply (unless otherwise noted)



G = 1, C_L = 1000pF

Figure 5-13. Small-Signal Step Response



G = 1, C_L = 100pF

Figure 5-14. Large-Signal Step Response

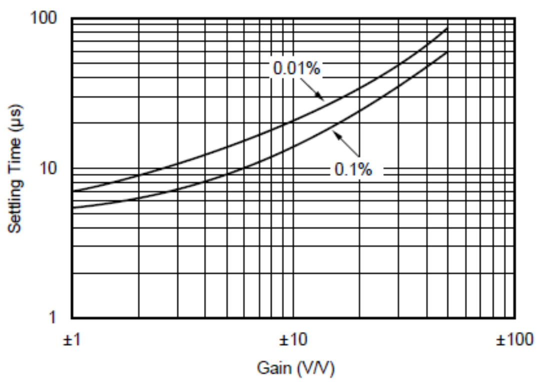


Figure 5-15. Settling Time vs Gain

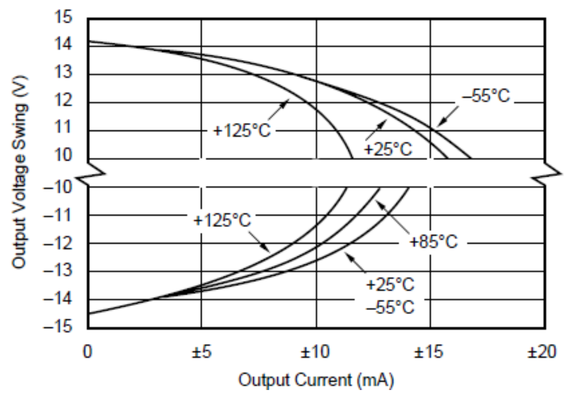


Figure 5-16. Output Voltage Swing vs Output Current

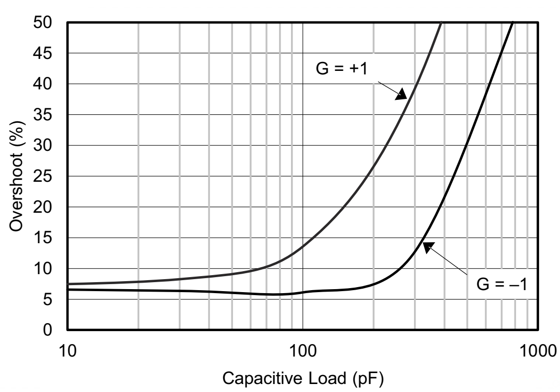


Figure 5-17. Small-Signal Overshoot vs Load Capacitance

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPAx130 series of op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power supply pins with 10nF ceramic capacitors or larger.

The OPAx130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPAx130 series of op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, and normal behavior can be expected when one amplifier in a package is overdriven or short-circuited.

6.1.1 Operating Voltage

The OPAx130 op amps operate with power supplies from ±2.25V to ±18V with excellent performance. Although specifications are production tested with ±15V supplies, most behavior remains unchanged throughout the full operating voltage range. See Section 5.7 for parameters that vary significantly with operating voltage.

6.1.2 Offset Voltage Trim

The offset voltage of the OPAx130 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx130 provide less than ±1mV of input offset voltage and less than 10µV/°C of input offset voltage drift over the operating temperature range.

6.1.3 Input Bias Current

Figure 5-5 shows that the input bias current of the OPAx130 is approximately 5pA at room temperature and increases with temperature.

Input stage cascode circuitry allows the input bias current to remain virtually unchanged throughout the full input common-mode range of the OPAx130. See also Figure 5-6.

6.2 Typical Application

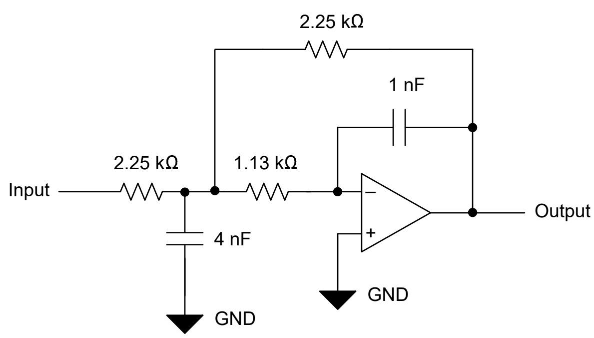


Figure 6-1. Second-Order Low-Pass Filter

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2006) to Revision B (May 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout document....................... 1
- Deleted DIP packages from data sheet...1
- Updated open-loop gain to match *Electrical Characteristics* in *Features* 1
- Added *Applications* 1
- Updated pin diagrams, added pin function tables, and moved all to new *Pin Configuration and Functions* 3
- Updated input voltage in *Absolute Maximum Ratings* 5
- Added input current and related footnote to *Absolute Maximum Ratings* 5
- Added *Recommended Operating Conditions* and *Thermal Information* 5
- Changed format of *Electrical Characteristics* to latest standard..7
- Updated nominal conditions in the header of *Electrical Characteristics* 7
- Deleted channel separation specification...7
- Updated common-mode voltage...7
- Updated common-mode rejection ratio and common-mode input impedance test conditions...........................7
- Changed differential input impedance from $10^{13}\Omega$ || 1pF to $10^{13}\Omega$ || 5pF...7
- Changed common-mode input impedance from $10^{13}\Omega$ || 3pF to $10^{13}\Omega$ || 4.3pF..7
- Updated open loop voltage gain MIN and TYP values for R_L = 10kΩ and R_L = 2kΩ..7
- Updated settling time test condition..7
- Moved voltage output negative MIN values to MAX values.. 7
- Changed capacitive load drive specification from 10nF to See *Typical Characteristics* 7

- Deleted note 1 from *Electrical Characteristics* 7
- Deleted Figure 5-7, *A_{OL}, CMR, PSR vs Temperature* 8
- Updated Figure 5-17, *Small-Signal Overshoot vs Load Capacitance* 8
- Updated text in *Offset Voltage Trim* 11
- Changed Figure 1, *OPA130 Offset Voltage Trim Circuit*, to Figure 6-1, *Second-Order Low-Pass Filter* 11

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA130UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA	Samples
OPA130UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	(O130, OPA) 130UA	Samples
OPA2130UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)	Samples
OPA2130UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	(2130UA, OPA)	Samples
OPA4130UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4130UA	Samples
OPA4130UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4130UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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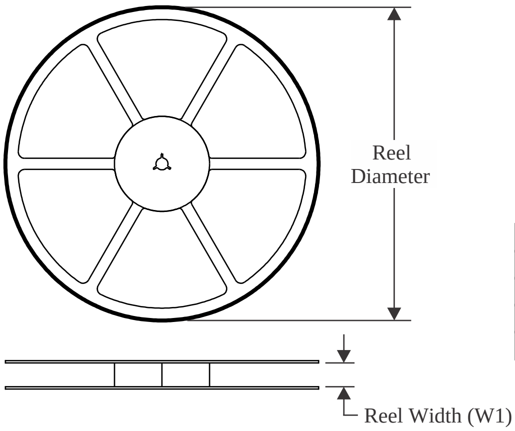
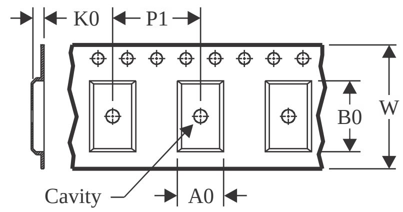
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

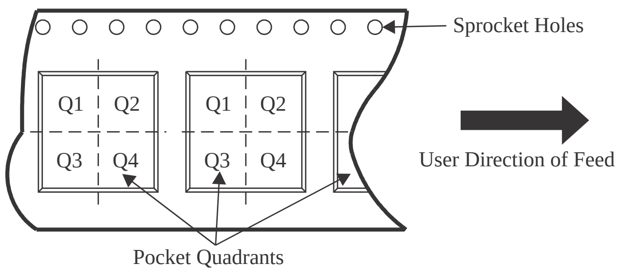


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

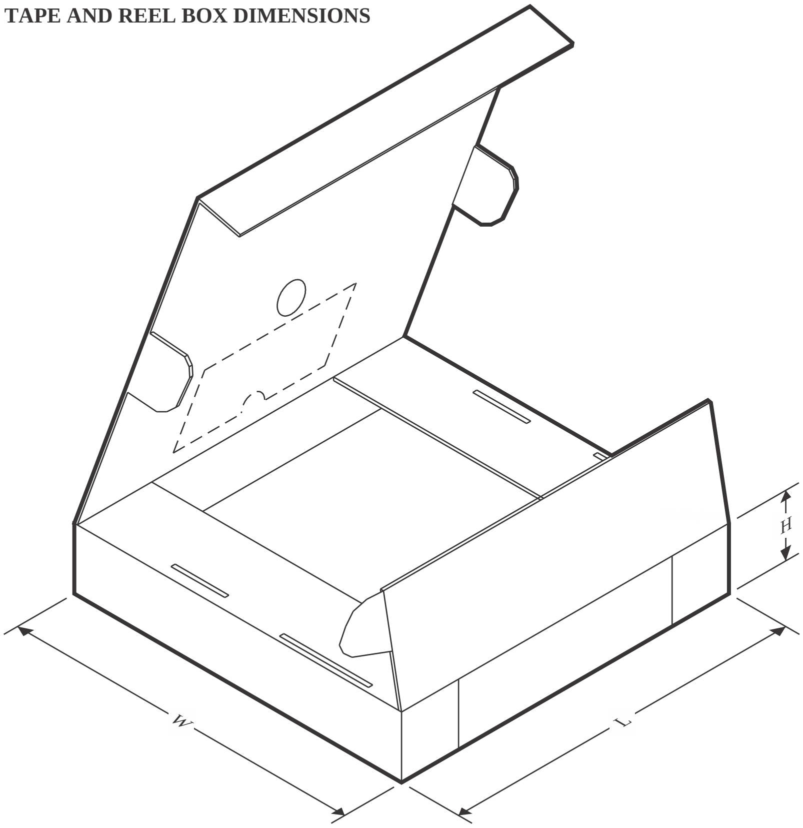
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4130UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

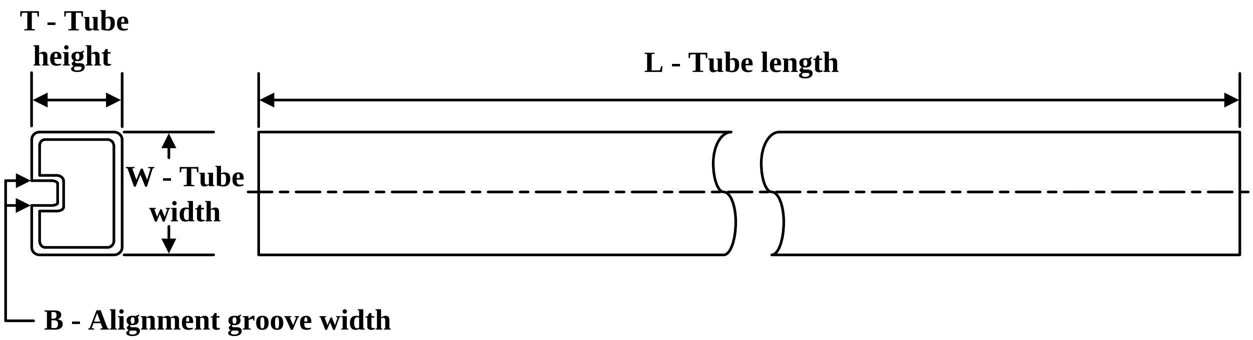
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

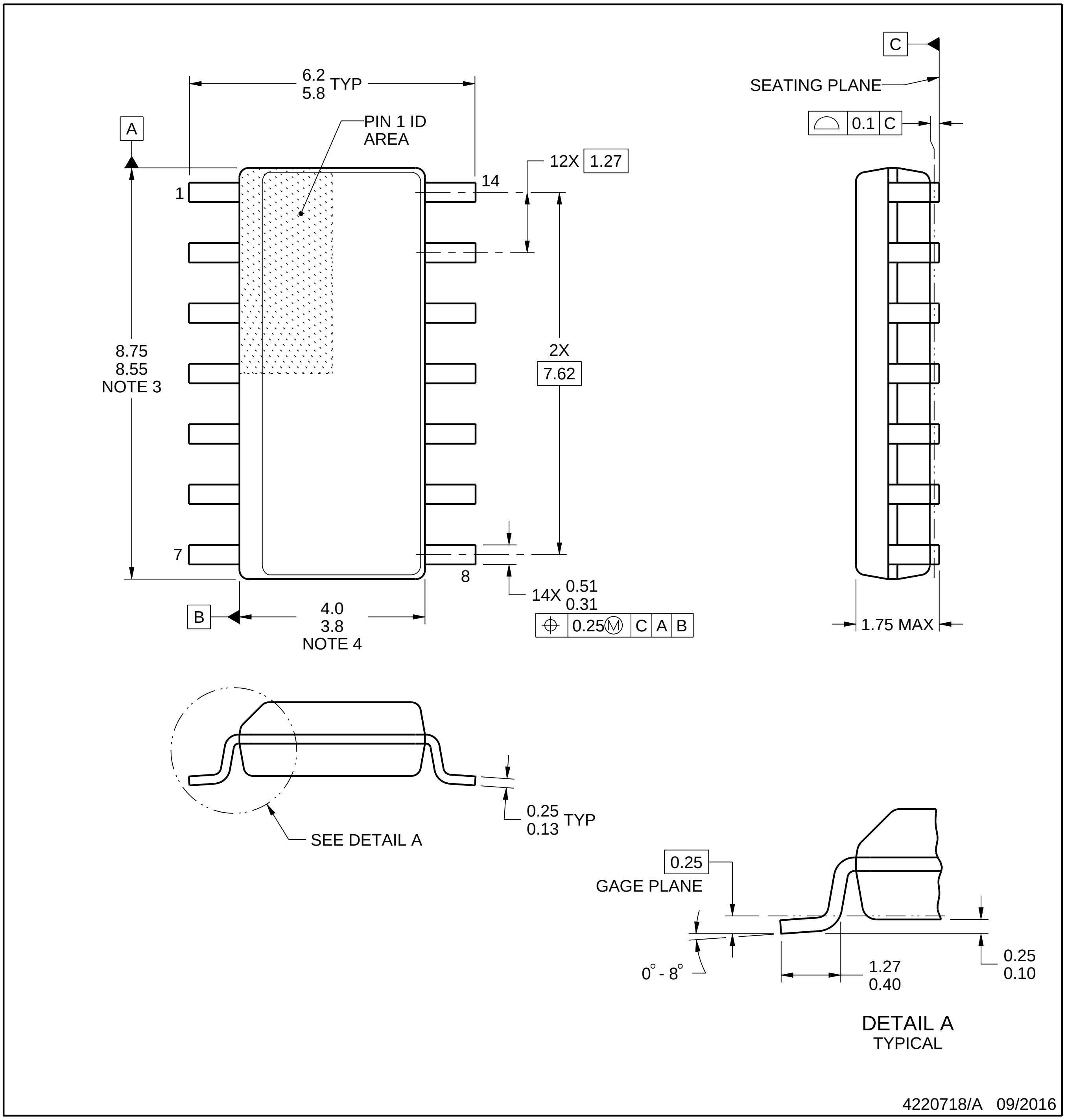
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA130UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2130UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2130UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4130UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



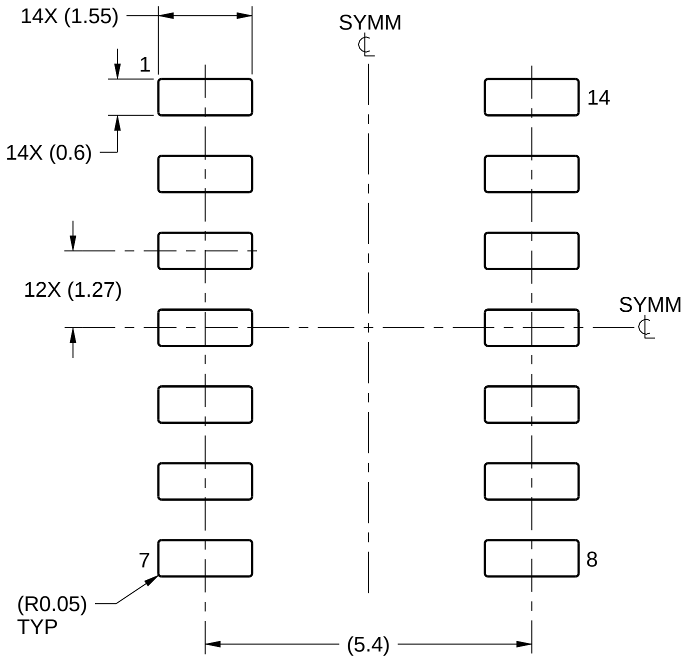
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2130UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4130UA	D	SOIC	14	50	506.6	8	3940	4.32

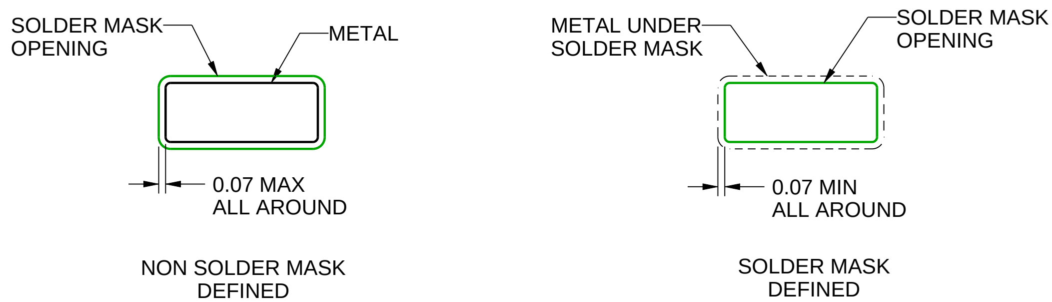


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

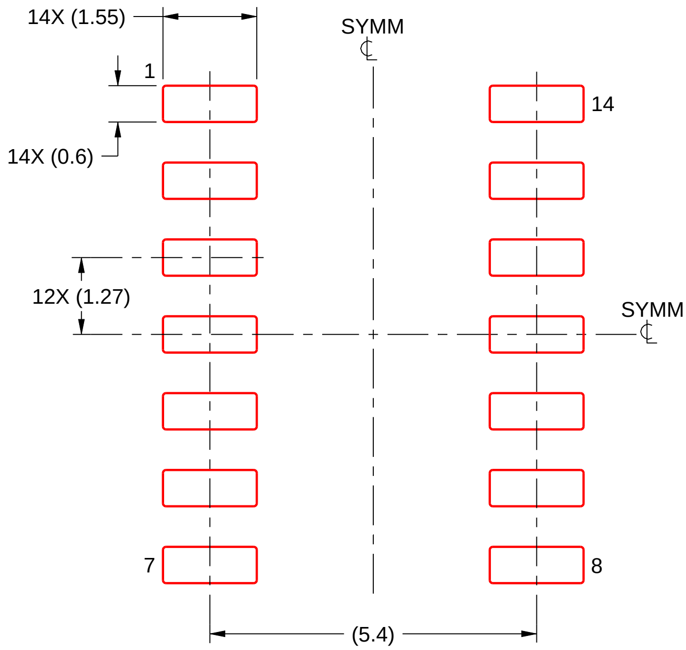


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

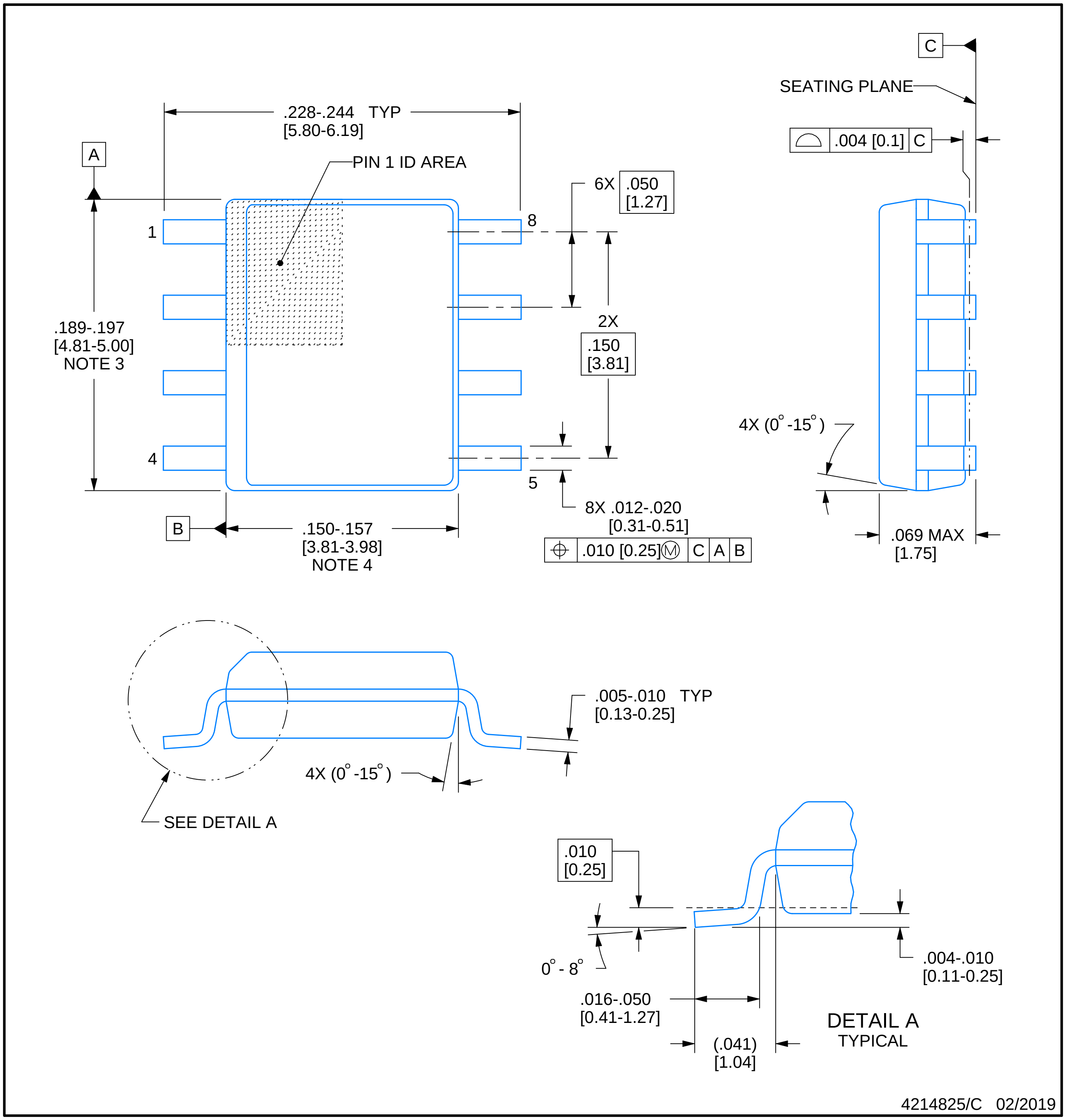


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

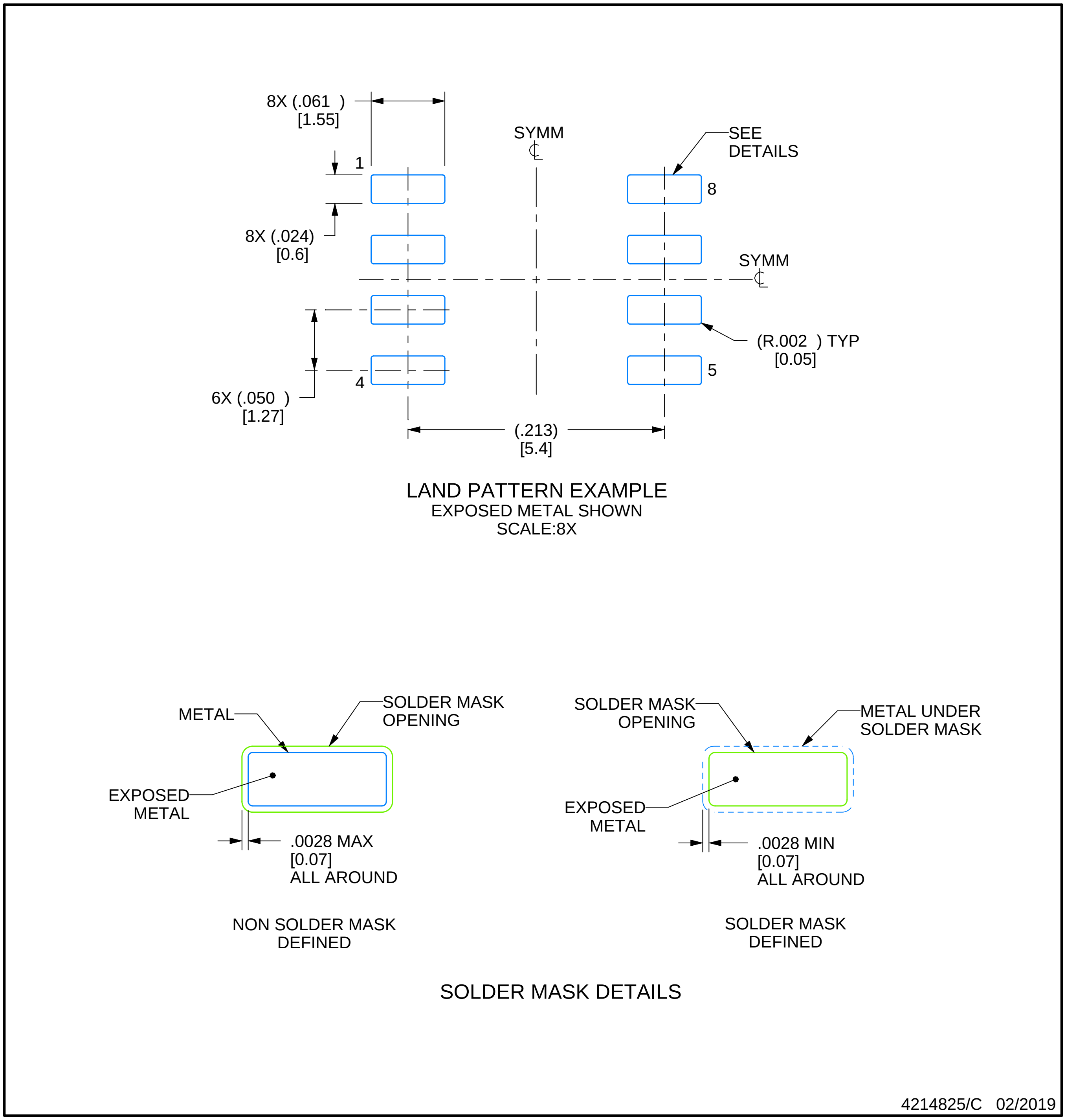
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



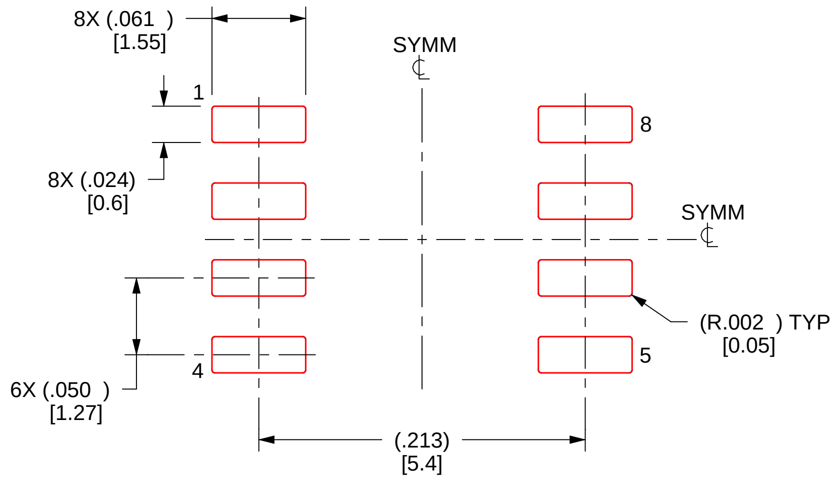
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.