



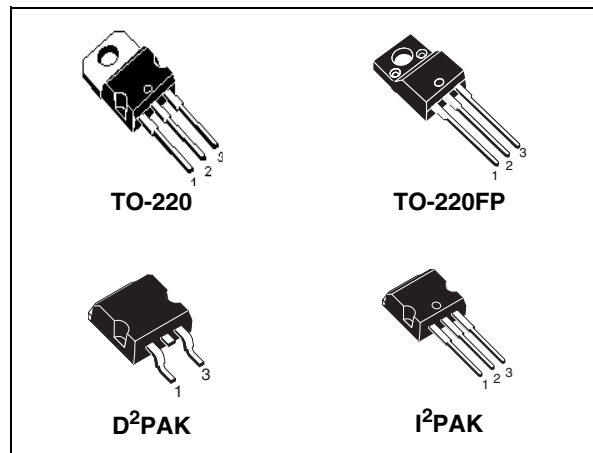
# STP7NK80Z - STP7NK80ZFP STB7NK80Z - STB7NK80Z-1

N-channel 800V - 1.5Ω - 5.2A - TO-220/TO-220FP/D<sup>2</sup>PAK/I<sup>2</sup>PAK  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>
STP7NK80Z	800V	< 1.8Ω	5.2A
STP7NK80ZFP	800V	< 1.8Ω	5.2A
STB7NK80Z	800V	< 1.8Ω	5.2A
STB7NK80Z-1	800V	< 1.8Ω	5.2A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



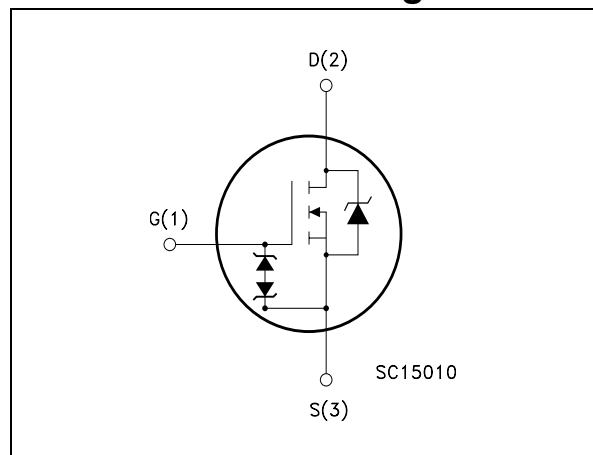
## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP7NK80Z	P7NK80Z	TO-220	Tube
STP7NK80ZFP	P7NK80ZFP	TO-220FP	Tube
STB7NK80ZT4	B7NK80Z	D <sup>2</sup> PAK	Tape e reel
STB7NK80Z-1	B7NK80Z-1	I <sup>2</sup> PAK	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>5</b>
	2.1 Electrical characteristics (curves) .....	7
<b>3</b>	<b>Test circuit</b> .....	<b>10</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>11</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>16</b>
<b>6</b>	<b>Revision history</b> .....	<b>17</b>

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 / D <sup>2</sup> PAK I <sup>2</sup> PAK	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	800		V
V <sub>GS</sub>	Gate- source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	5.2	5.2 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100°C	3.3	3.3 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	20.8	20.8 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	125	30	W
	Derating factor	1	0.24	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; T <sub>C</sub> = 25°C)	--	2500	V
T <sub>j</sub>	Max operating junction temperature	-55 to 150		°C
T <sub>stg</sub>	Storage temperature			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 5.2 A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220/D <sup>2</sup> PAK I <sup>2</sup> PAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1	4.2	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5		°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300		°C

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	5.2	A
$E_{AS}$	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	210	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1MA, V_{GS} = 0$	800			V
$I_{DSS}$	Zero gate voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 2.6 A$		1.5	1.8	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15v, I_D = 2.6 A$		5		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1138 122 25		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0V, V_{DS} = 0V \text{ to } 640V$		50		pF
$t_{d(on)}$ $t_r$ $t_{r(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 400 V, I_D = 2.6 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <a href="#">Figure 16</a> )		20 12 45 20		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 640 V, I_D = 5.2 A,$ $V_{GS} = 10 V$ (see <a href="#">Figure 17</a> )		40 7 21	56	nC nC nC
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD} = 640 V, I_D = 5.2 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see <a href="#">Figure 16</a> )		12 10 20		ns ns ns

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				5.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.2 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		530		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50 \text{ V}, T_J = 150^\circ\text{C}$		3.31		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 21</a> )		12.5		A

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%
2. Pulse width limited by safe operating area

**Table 7. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/  
D<sup>2</sup>PAK/I<sup>2</sup>PAK

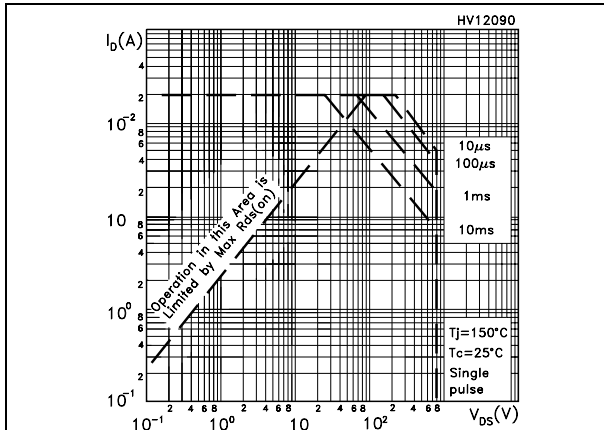


Figure 2. Thermal impedance for TO-220/  
D<sup>2</sup>PAK/I<sup>2</sup>PAK

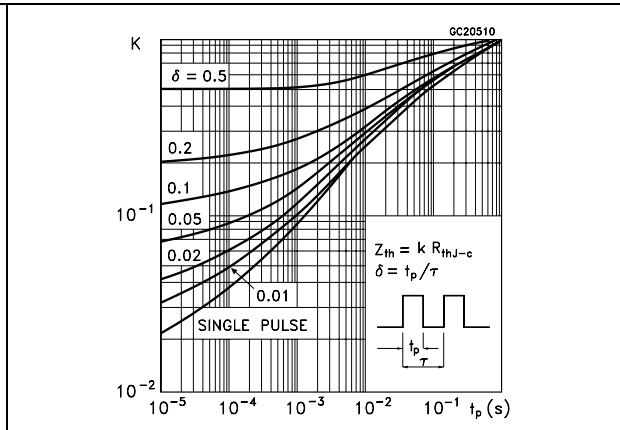


Figure 3. Safe operating area for TO-220FP

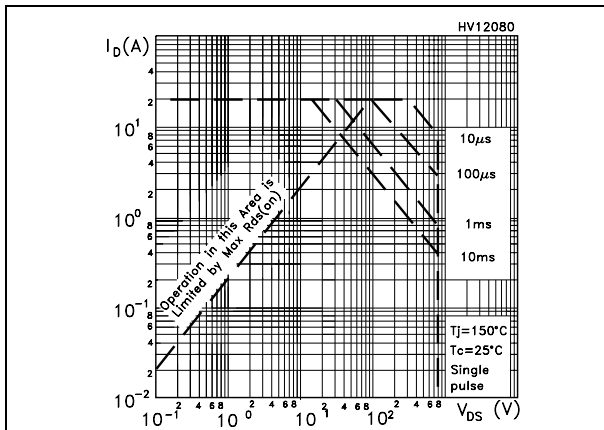


Figure 4. Thermal impedance for TO-220FP

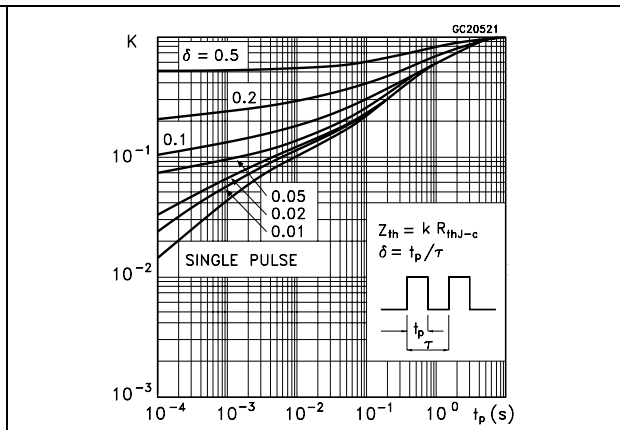


Figure 5. Output characteristics

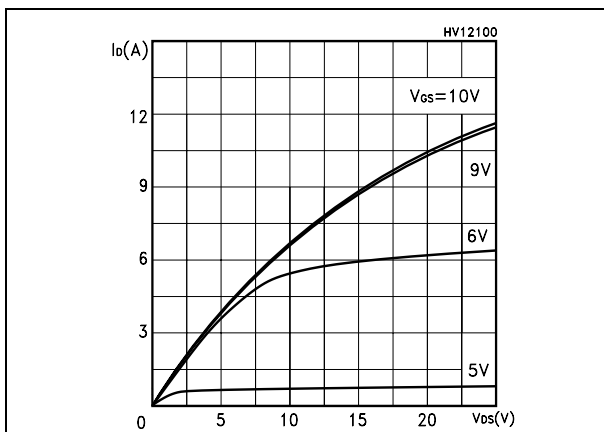


Figure 6. Transfer characteristics

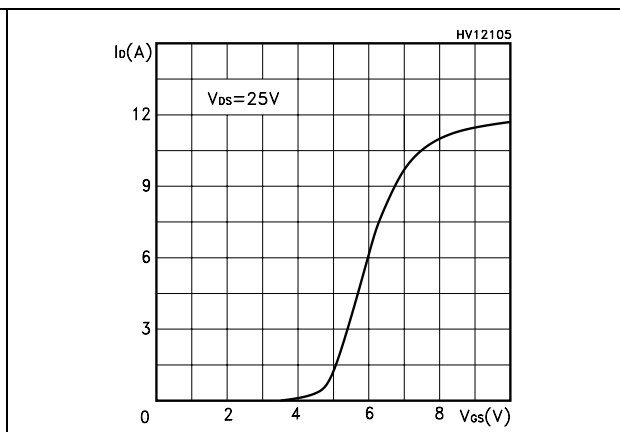


Figure 7. Transconductance

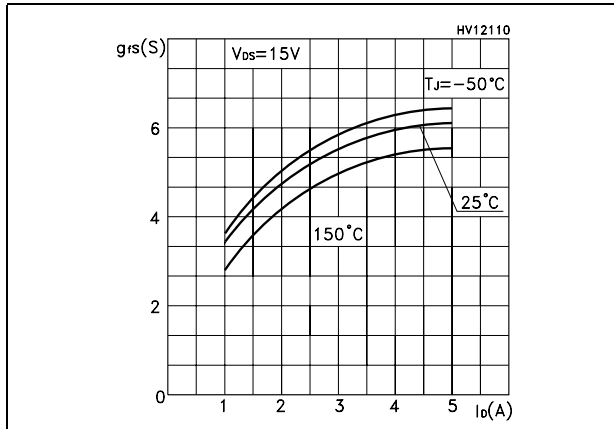


Figure 8. Static drain-source on resistance

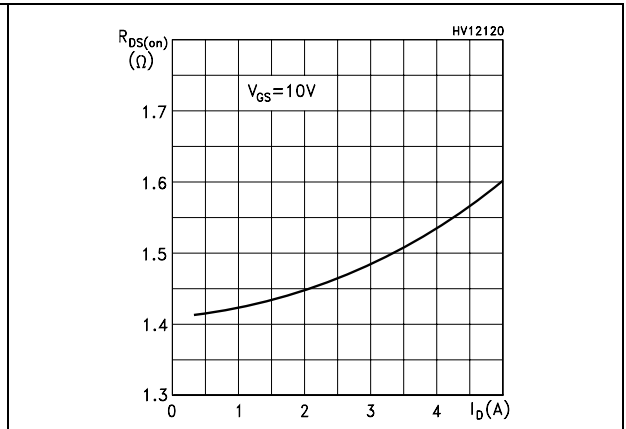


Figure 9. Gate charge vs gate-source voltage

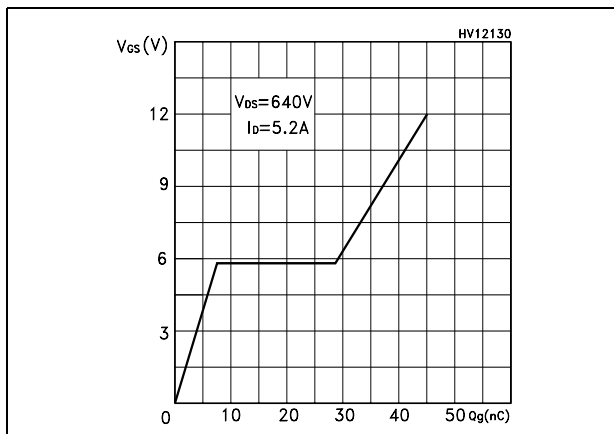


Figure 10. Capacitance variations

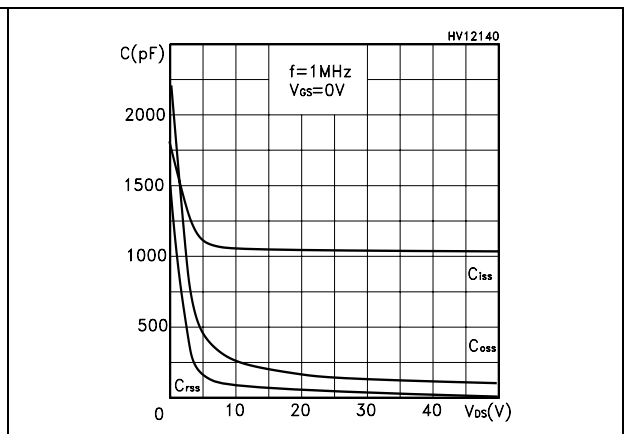


Figure 11. Normalized gate threshold voltage vs temperature

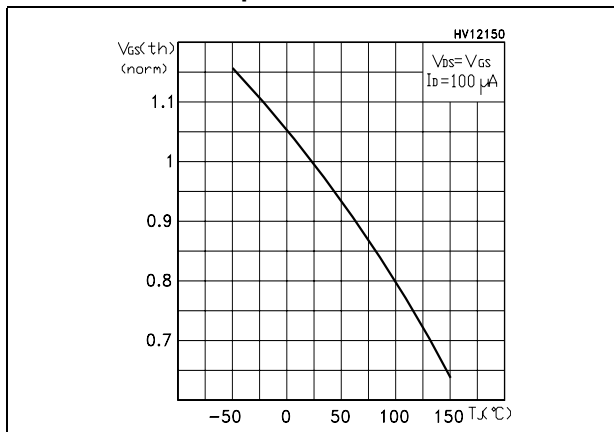


Figure 12. Normalized on resistance vs temperature

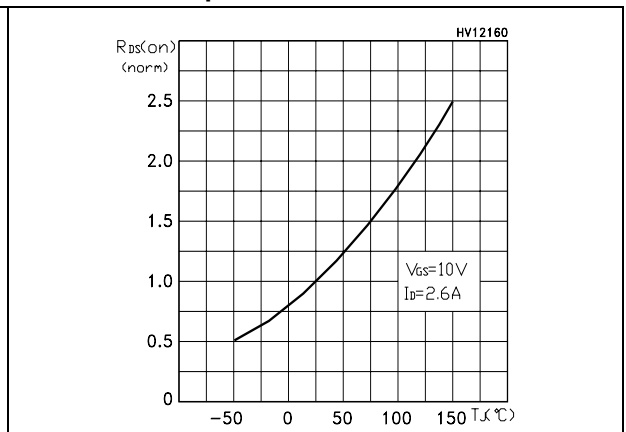




Figure 13. Source-drain diode forward characteristic

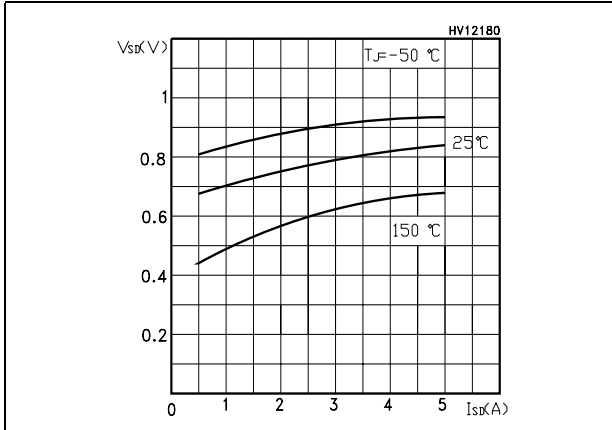


Figure 14. Normalized BVDSS vs temperature

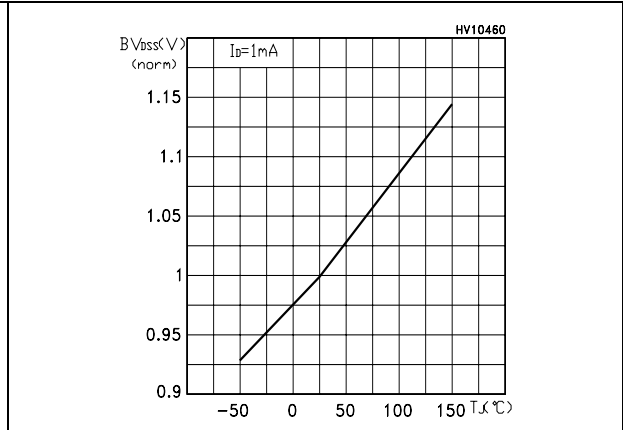
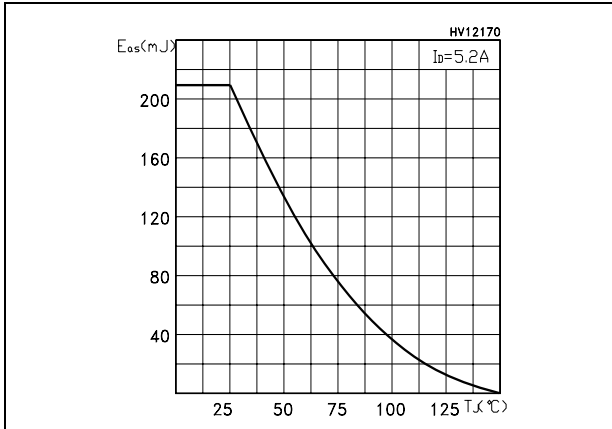


Figure 15. Maximum avalanche energy vs temperature



### 3 Test circuit

Figure 16. Switching times test circuit for resistive load

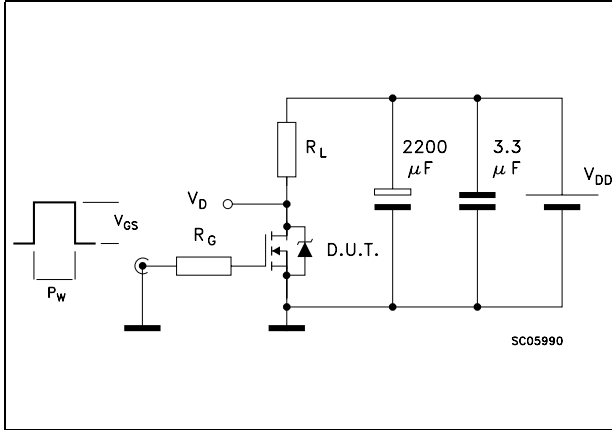


Figure 17. Gate charge test circuit

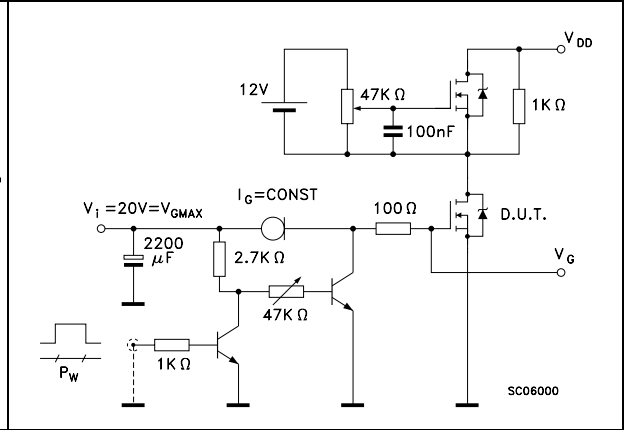


Figure 18. Test circuit for inductive load switching and diode recovery times

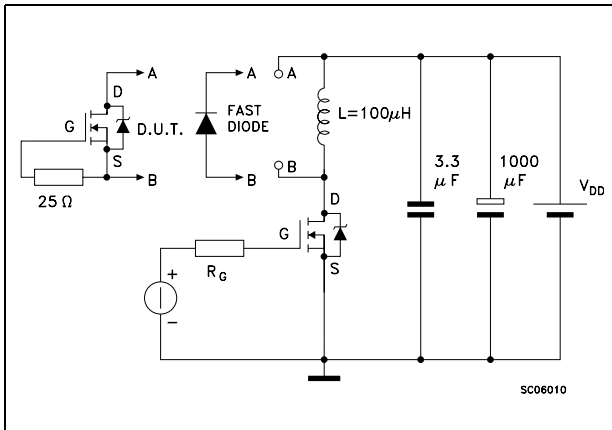


Figure 19. Unclamped Inductive load test circuit

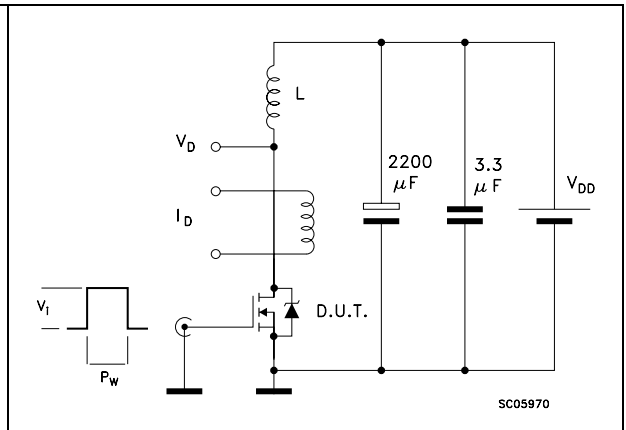


Figure 20. Unclamped inductive waveform

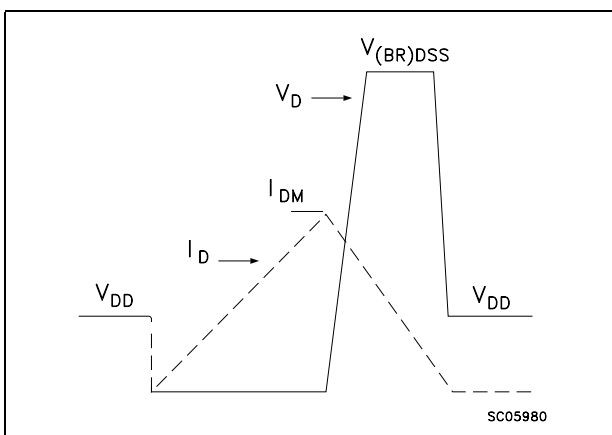
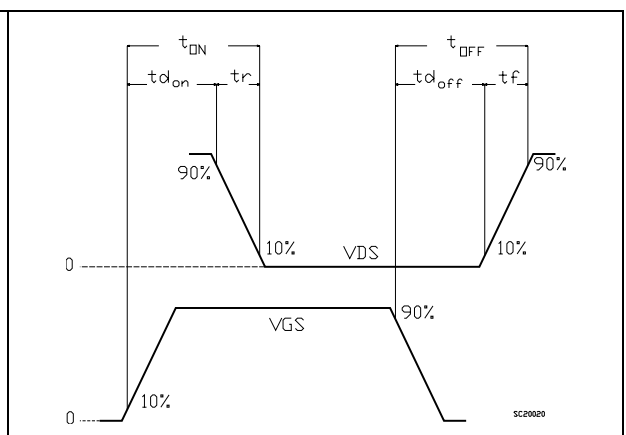


Figure 21. Switching time waveform

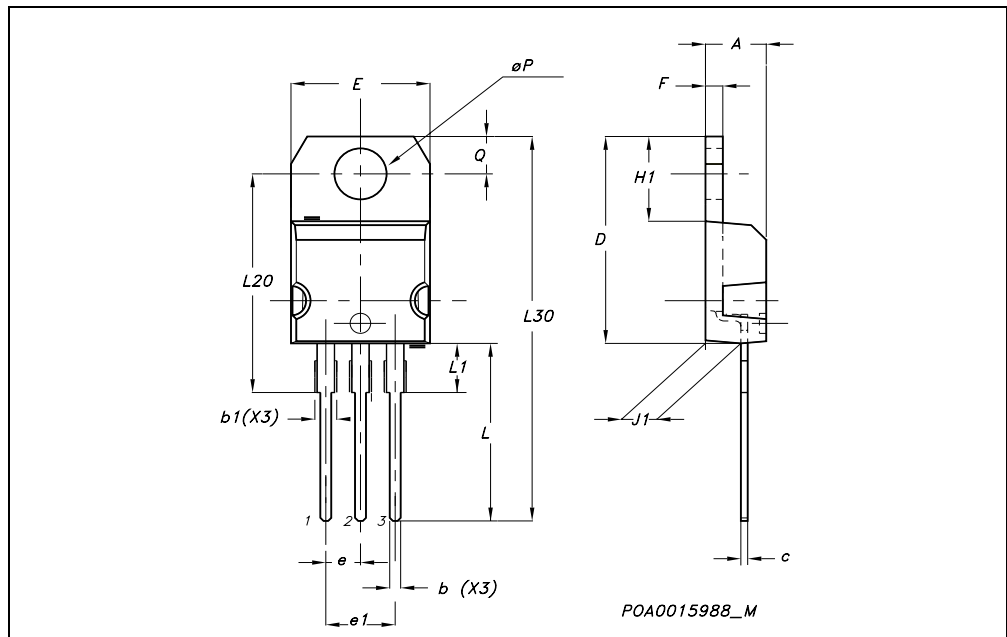


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

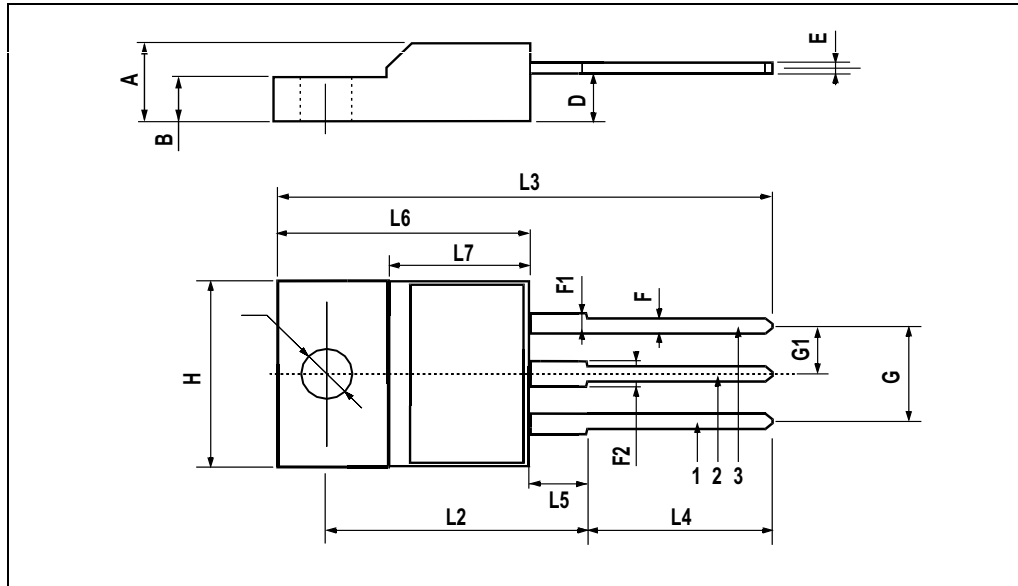
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



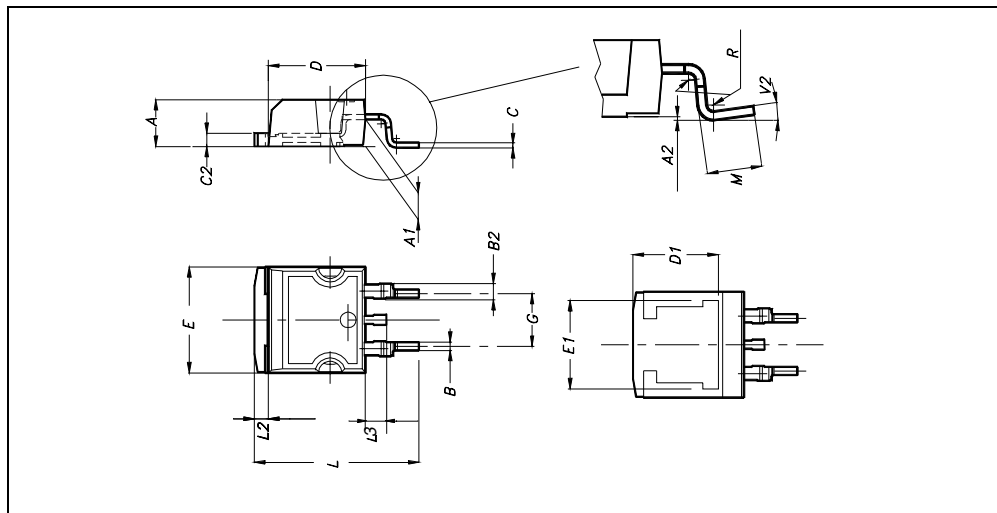
**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



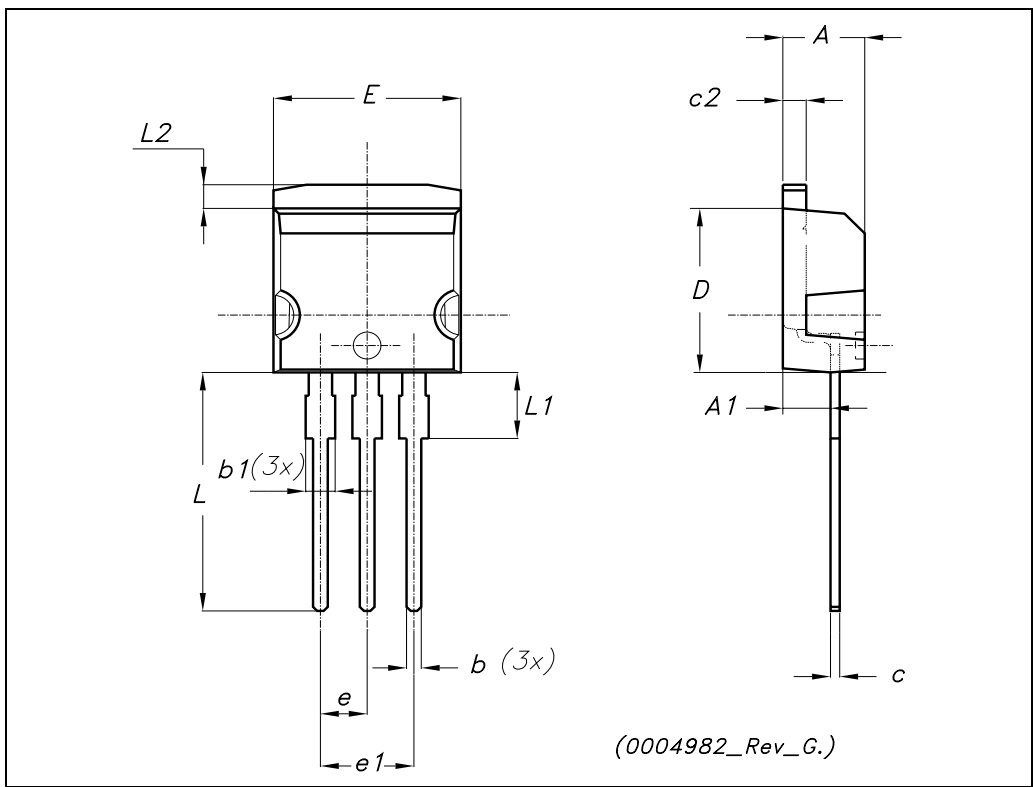
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



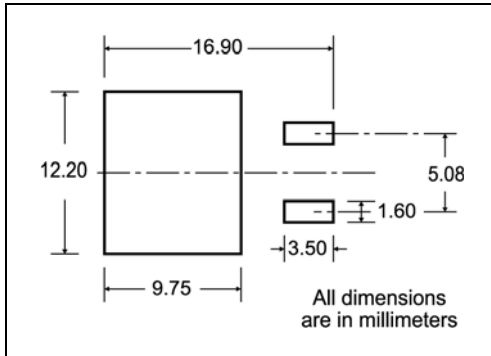
**TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



# 5 Packaging mechanical data

## D<sup>2</sup>PAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius

R min.

\* on sales type



## 6 Revision history

**Table 8. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
09-Sep-2004	3	Complete version
16-Aug-2006	4	New template, no content change
09-Oct-2006	5	Corrected order code

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)