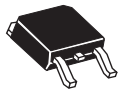


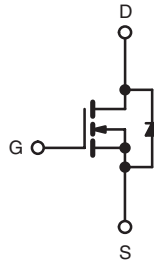
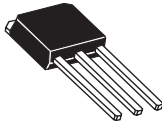
## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.54
$Q_g$ (Max.) (nC)	8.3	
$Q_{gs}$ (nC)	2.3	
$Q_{gd}$ (nC)	3.8	
Configuration	Single	

DPAK  
(TO-252)



IPAK  
(TO-251)



N-Channel MOSFET

### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR110/SiHFR110)
- Straight Lead (IRFU110/SiHFU110)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR110PbF	IRFR110TRLPbF <sup>a</sup>	IRFR110TRPbF <sup>a</sup>	IRFR110TRRPbF <sup>a</sup>	IRFU110PbF
	SiHFR110-E3	SiHFR110TL-E3 <sup>a</sup>	SiHFR110T-E3 <sup>a</sup>	SiHFR110TR-E3 <sup>a</sup>	SiHFU110-E3
SnPb	IRFR110	IRFR110TRL <sup>a</sup>	IRFR110TR <sup>a</sup>	-	IRFU110
	SiHFR110	SiHFR110TL <sup>a</sup>	SiHFR110T <sup>a</sup>	-	SiHFU110

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	100	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	4.3	A
		$T_C = 100\text{ }^\circ\text{C}$		2.7	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	17	W/ $^\circ\text{C}$
Linear Derating Factor				0.20	
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.020	
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	100	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	4.3	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	2.5	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	25	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	$T_A = 25\text{ }^\circ\text{C}$			2.5	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns

\* Pb containing terminations are not RoHS compliant, exemptions may apply

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	260 <sup>d</sup>	

### Notes

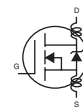
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 8.1\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 4.3\text{ A}$  (see fig. 12).
- $I_{SD} \leq 5.6\text{ A}$ ,  $dl/dt \leq 75\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).


<b>THERMAL RESISTANCE RATINGS</b>				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	5.0	

### Note

- When mounted on 1" square PCB (FR-4 or G-10 material).

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 2.6\text{ A}^b$	-	-	0.54	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 2.6\text{ A}$	1.6	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5	-	180	-	pF
Output Capacitance	$C_{oss}$		-	80	-	
Reverse Transfer Capacitance	$C_{riss}$		-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 5.6\text{ A}$ , $V_{DS} = 80\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	8.3	nC
Gate-Source Charge	$Q_{gs}$		-	-	2.3	
Gate-Drain Charge	$Q_{gd}$		-	-	3.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$ , $I_D = 5.6\text{ A}$ , $R_G = 24\text{ }\Omega$ , $R_D = 8.4\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	6.9	-	ns
Rise Time	$t_r$		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	
Fall Time	$t_f$		-	9.4	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	



SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	4.3	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	17	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 4.3\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 5.6\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	100	200	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.44	0.88	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

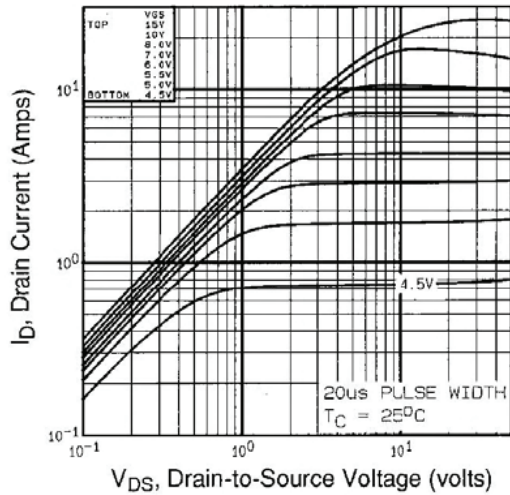


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

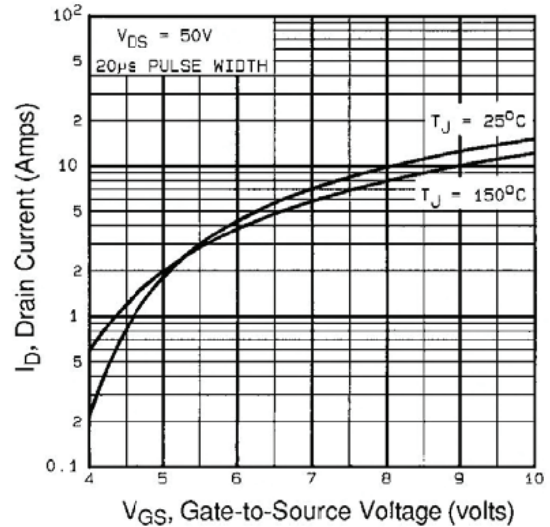


Fig. 3 - Typical Transfer Characteristics

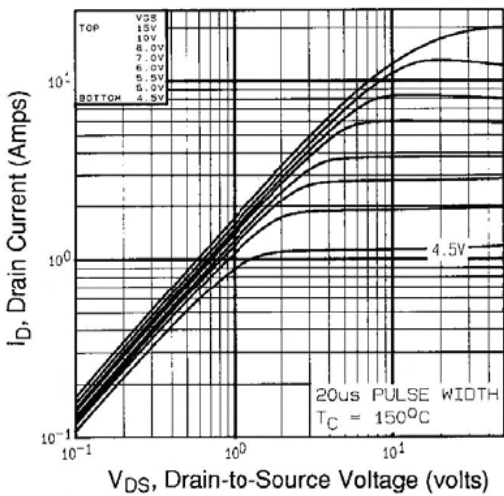


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

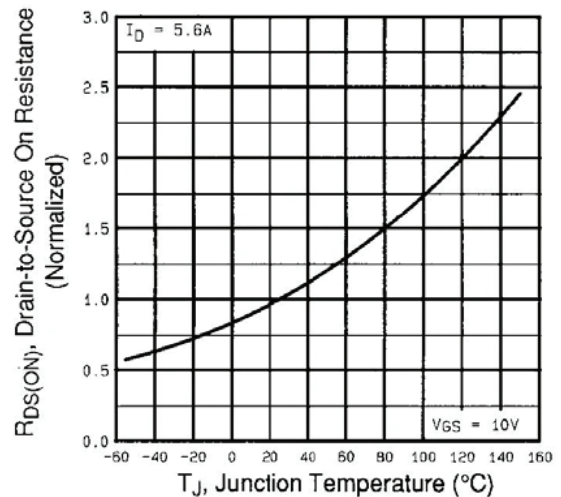


Fig. 4 - Normalized On-Resistance vs. Temperature

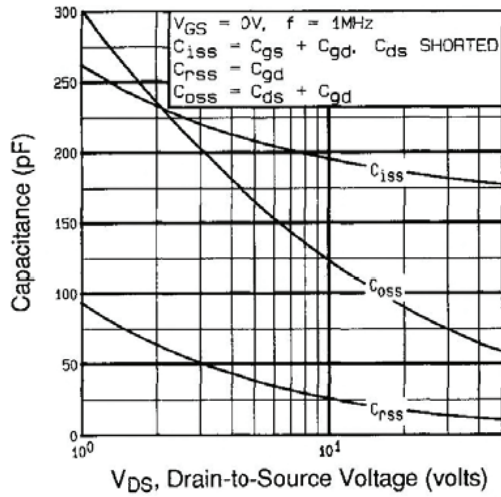


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

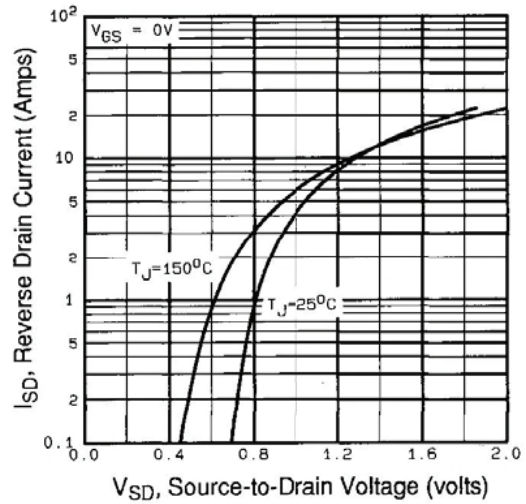


Fig. 7 - Typical Source-Drain Diode Forward Voltage

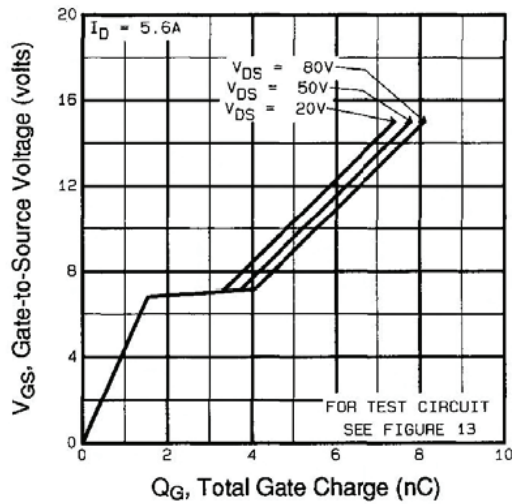


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

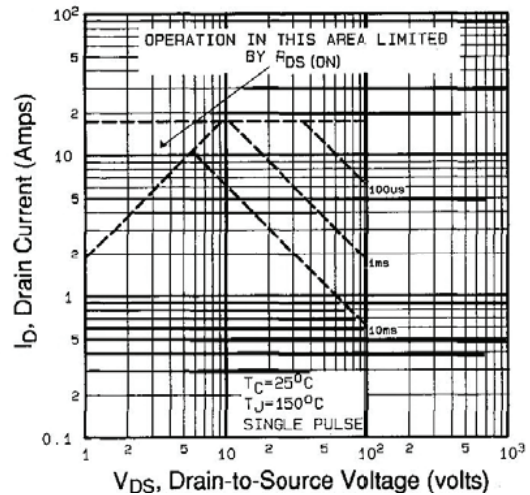


Fig. 8 - Maximum Safe Operating Area

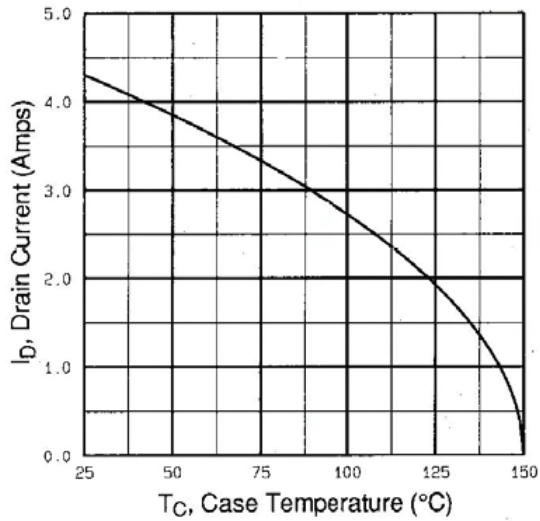


Fig. 9 - Maximum Drain Current vs. Case Temperature

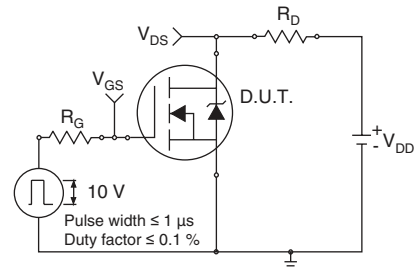


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

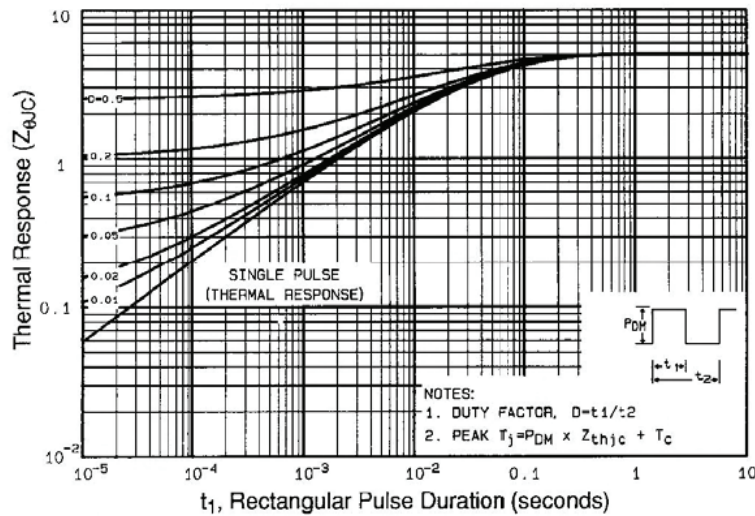


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

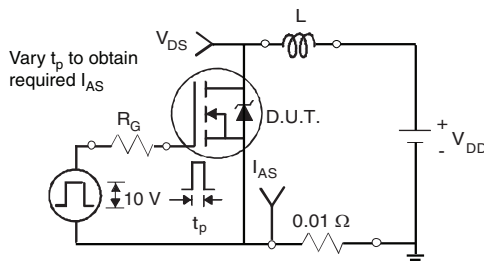


Fig. 12a - Unclamped Inductive Test Circuit

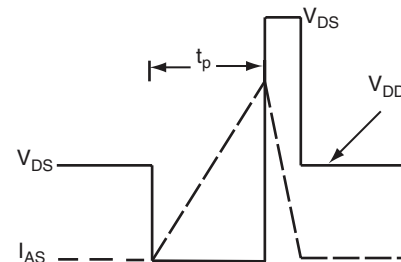


Fig. 12b - Unclamped Inductive Waveforms

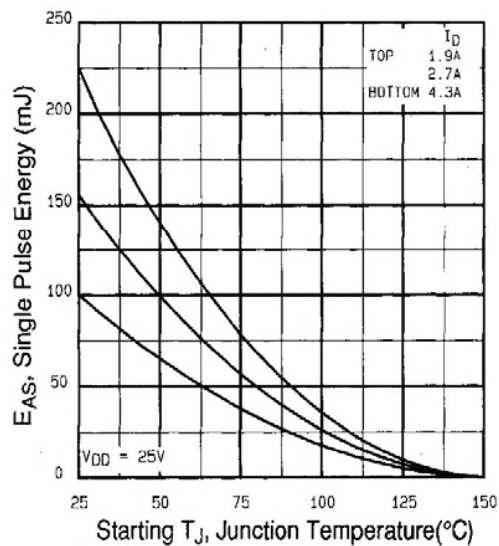


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

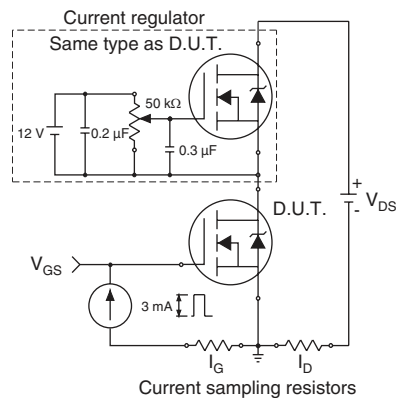


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit

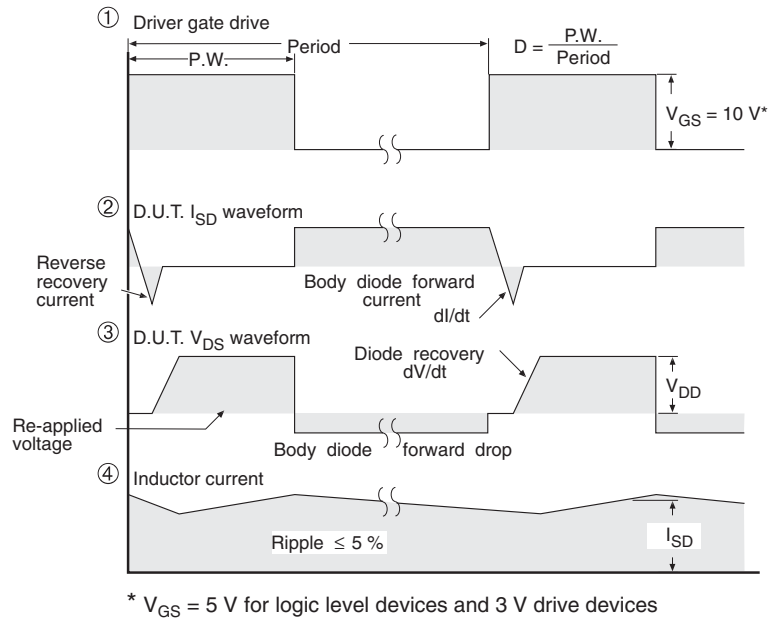
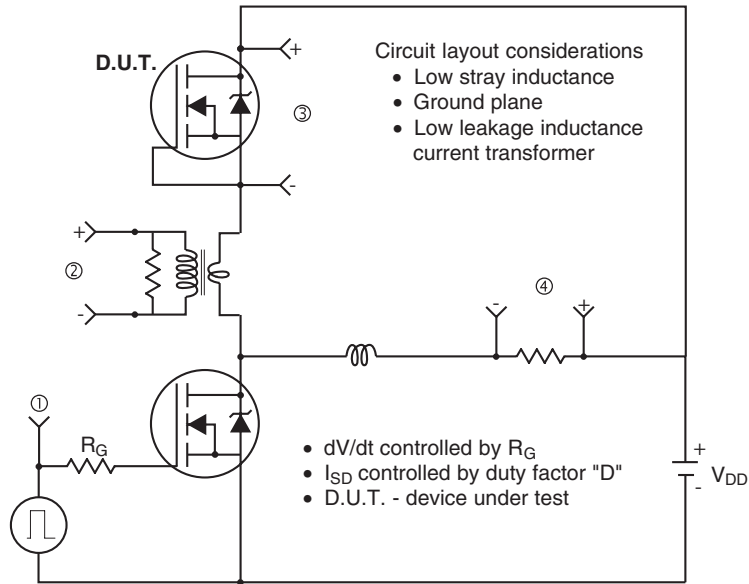


Fig. 14 -For N-Channel

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