

Typical Applications

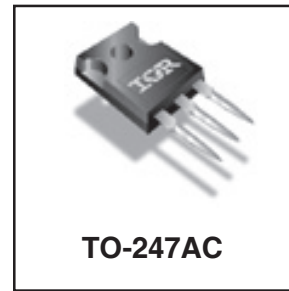
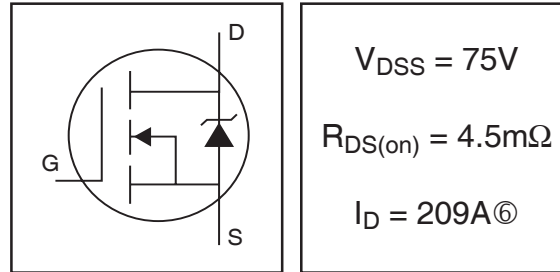
- Integrated Starter Alternator
- 42 Volts Automotive Electrical Systems
- Lead-Free

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



Absolute Maximum Ratings

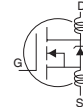
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	209Ⓢ	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	148Ⓢ	
I_{DM}	Pulsed Drain Current ①	840	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	470	W
	Linear Derating Factor	3.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche EnergyⓉ	1970	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche EnergyⓉ		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.32	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.085	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	3.6	4.5	mΩ	V _{GS} = 10V, I _D = 125A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = 10V, I _D = 250μA
g _{fs}	Forward Transconductance	130	—	—	S	V _{DS} = 25V, I _D = 125A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V
Q _g	Total Gate Charge	—	410	620	nC	I _D = 125A
Q _{gs}	Gate-to-Source Charge	—	92	140		V _{DS} = 60V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	140	210		V _{GS} = 10V ④
t _{d(on)}	Turn-On Delay Time	—	23	—	ns	V _{DD} = 38V
t _r	Rise Time	—	190	—		I _D = 125A
t _{d(off)}	Turn-Off Delay Time	—	130	—		R _G = 1.2Ω
t _f	Fall Time	—	130	—		V _{GS} = 10V ④
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	13	—		
C _{iss}	Input Capacitance	—	13000	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	2100	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	500	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	9780	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	1360	—		V _{GS} = 0V, V _{DS} = 60V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	2320	—		V _{GS} = 0V, V _{DS} = 0V to 60V



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	209⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	840		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 125A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	140	210	ns	T _J = 25°C, I _F = 125A
Q _{rr}	Reverse Recovery Charge	—	880	1320	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T_J = 25°C, L = 0.25mH
R_G = 25Ω, I_{AS} = 125A. (See Figure 12).
- ③ I_{SD} ≤ 125A, di/dt ≤ 260A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 90A.
- ⑦ Limited by T_{Jmax}, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

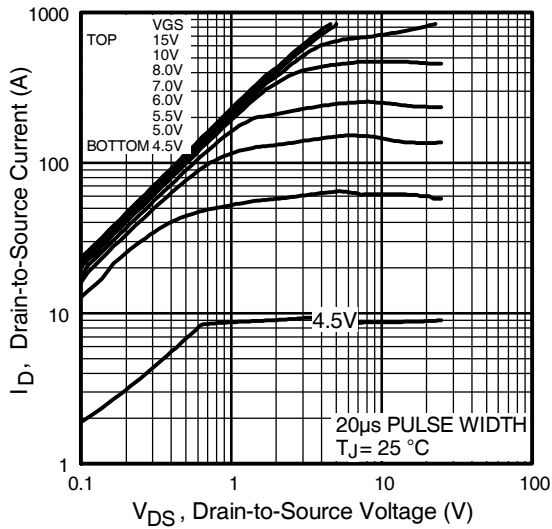


Fig 1. Typical Output Characteristics

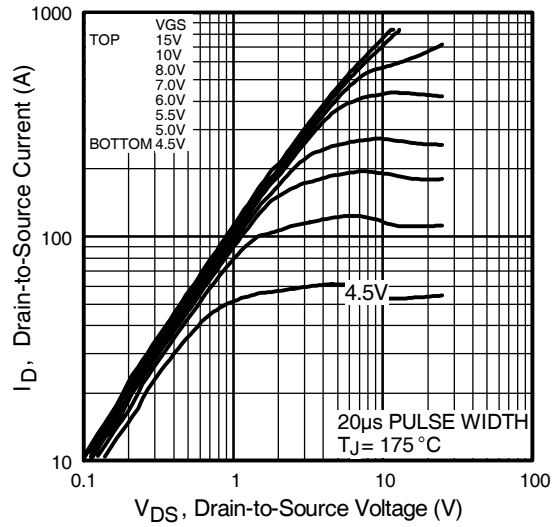


Fig 2. Typical Output Characteristics

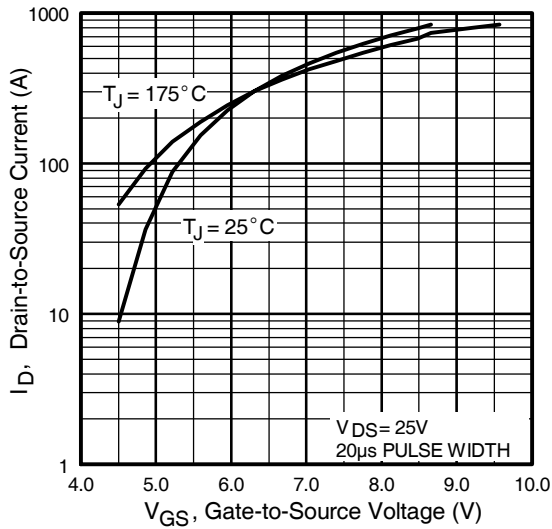


Fig 3. Typical Transfer Characteristics

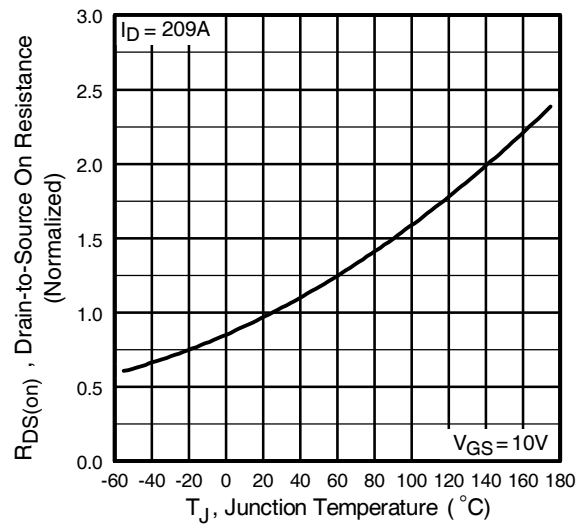


Fig 4. Normalized On-Resistance Vs. Temperature

IRFP2907PbF

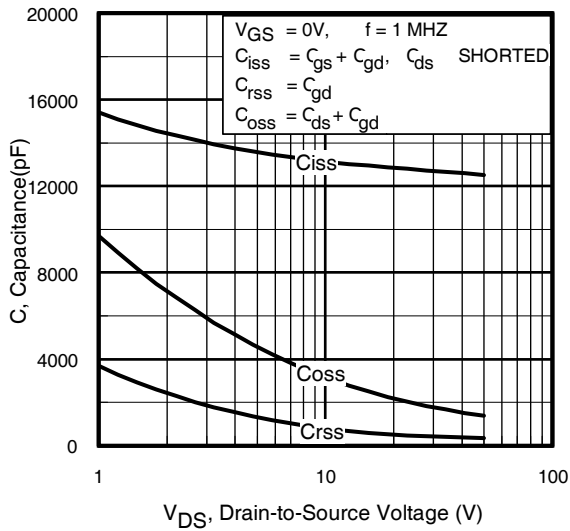


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

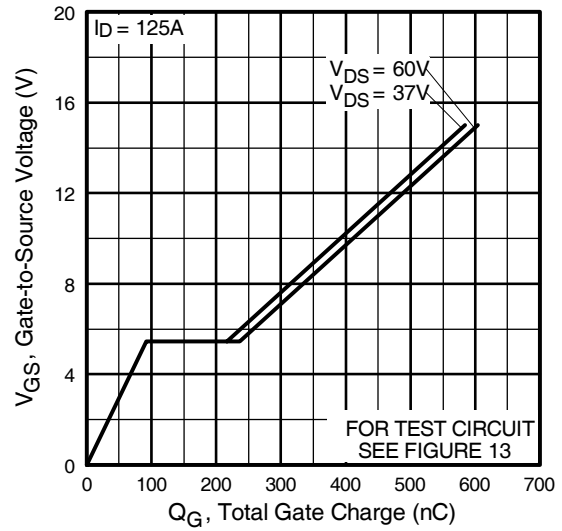


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

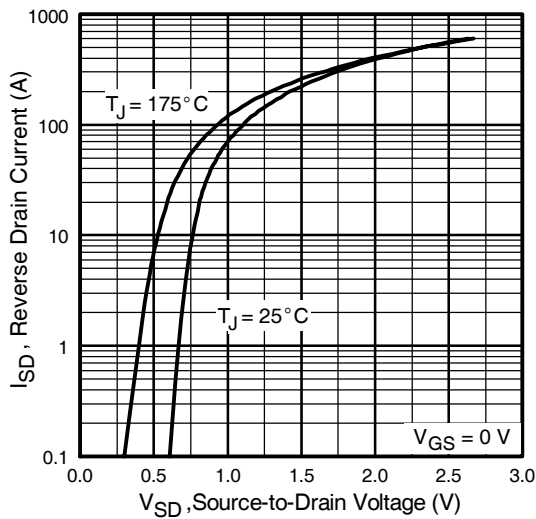


Fig 7. Typical Source-Drain Diode Forward Voltage

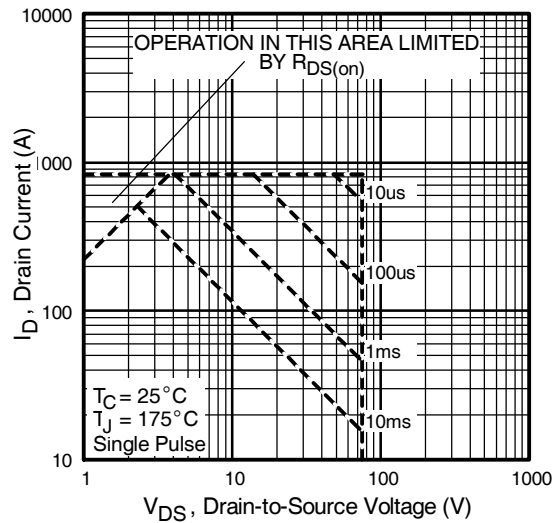


Fig 8. Maximum Safe Operating Area

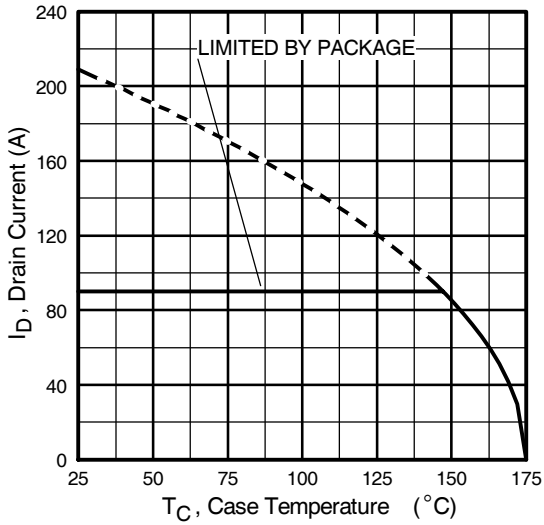


Fig 9. Maximum Drain Current Vs. Case Temperature

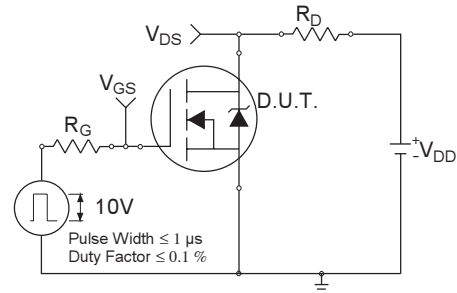


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

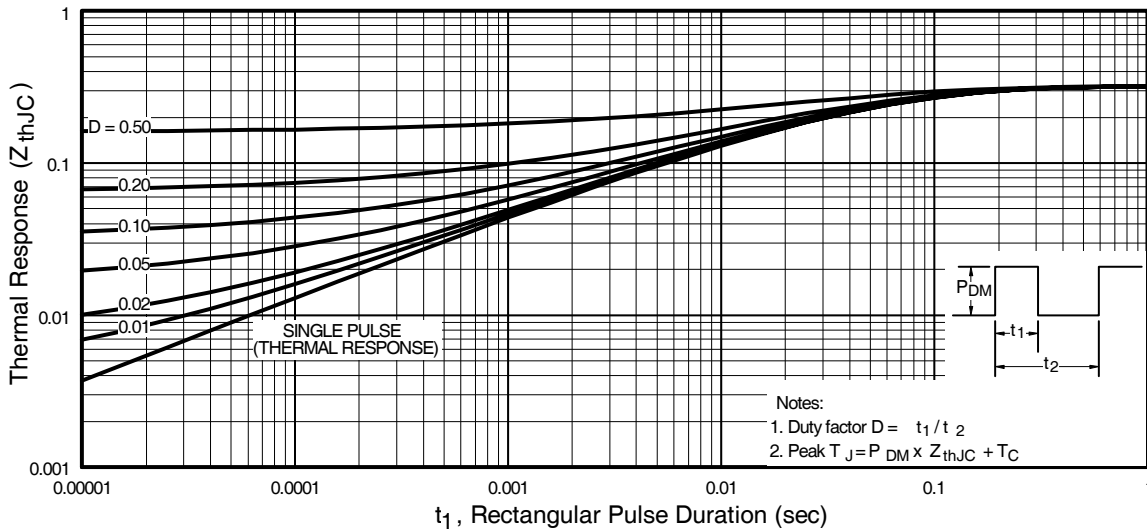


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFP2907PbF

International
IR Rectifier

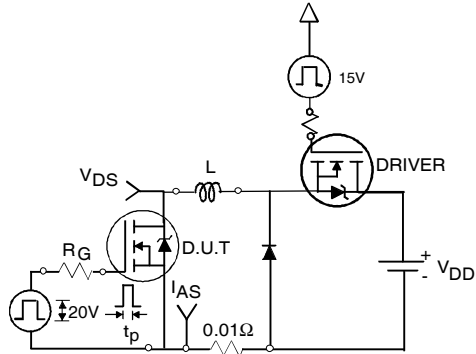


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform

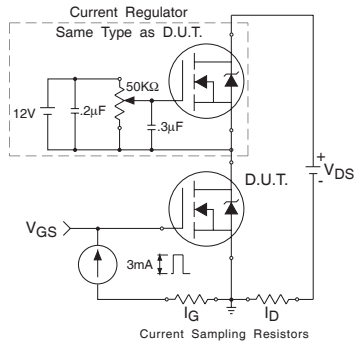


Fig 13b. Gate Charge Test Circuit

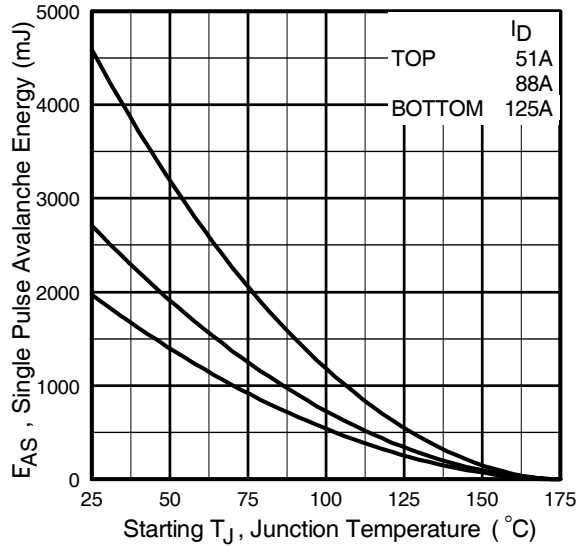


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

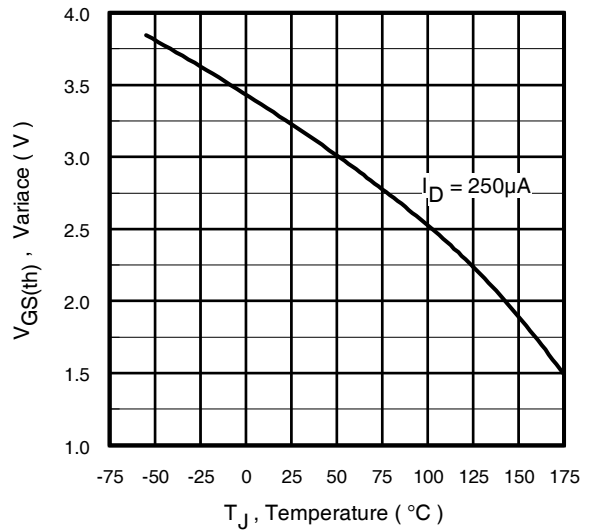


Fig 14. Threshold Voltage Vs. Temperature

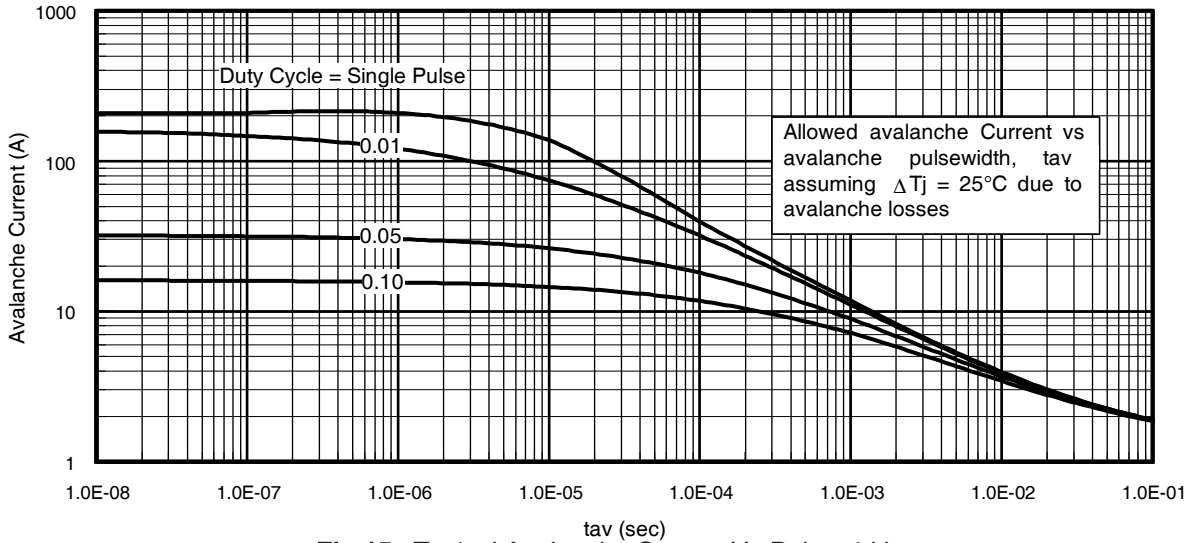


Fig 15. Typical Avalanche Current Vs.Pulsewidth

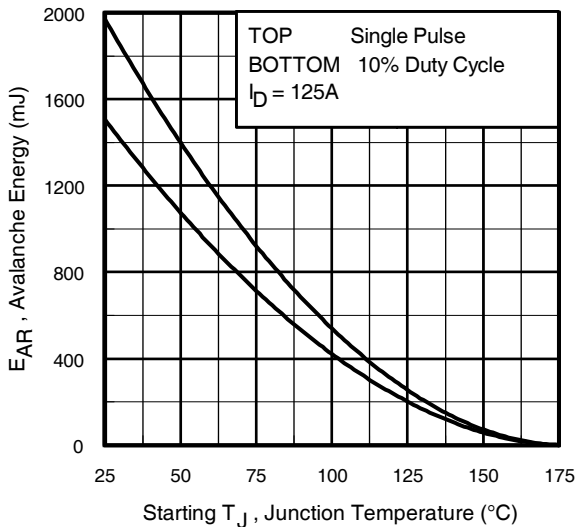


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

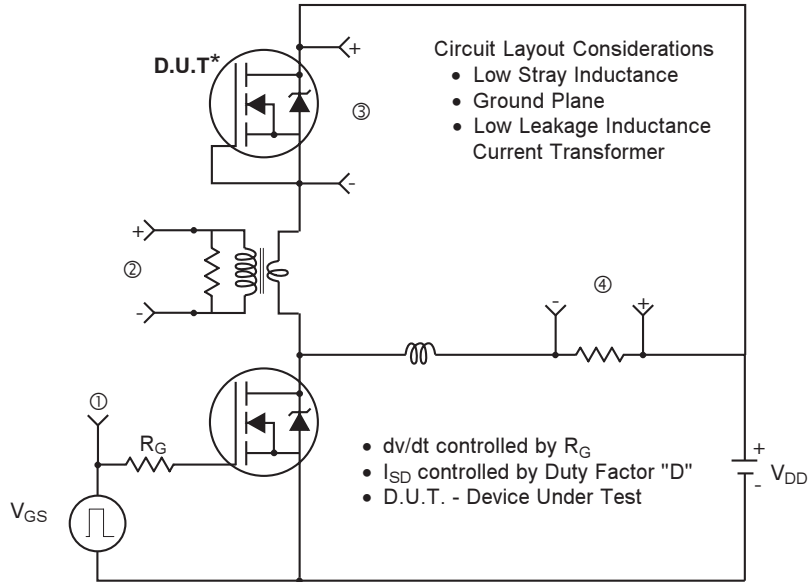
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

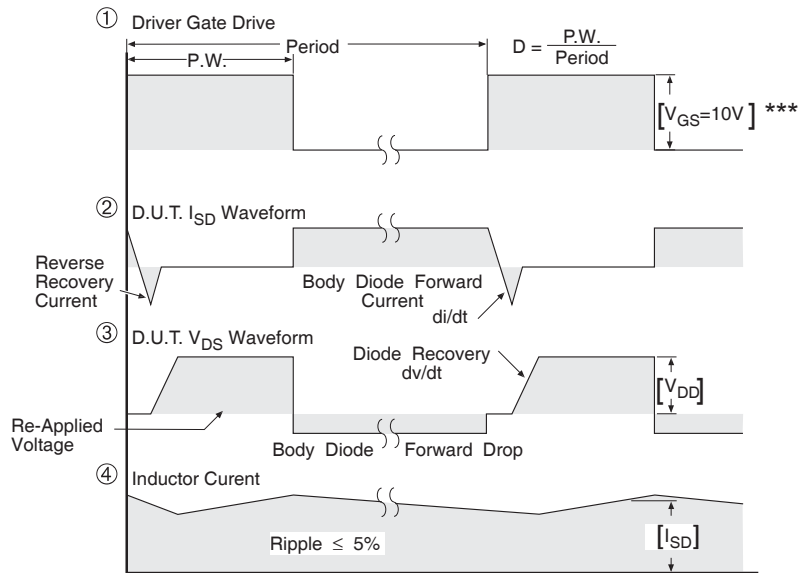
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

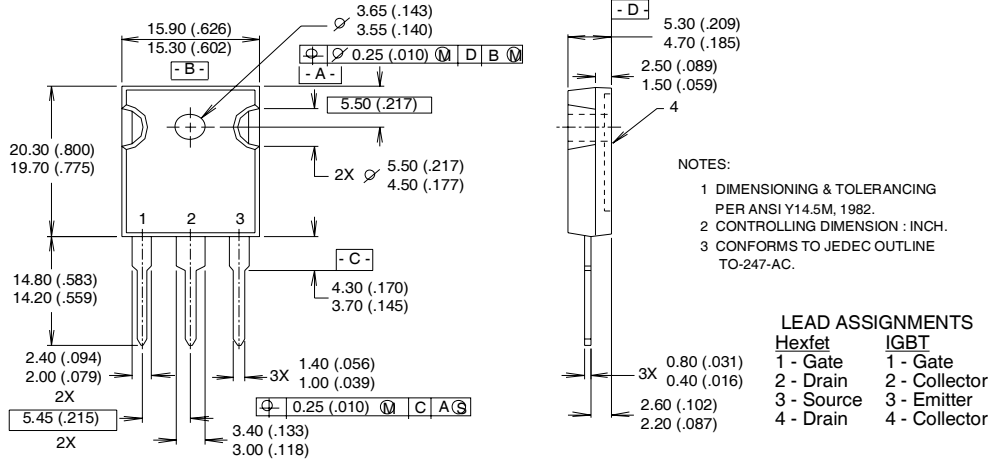


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

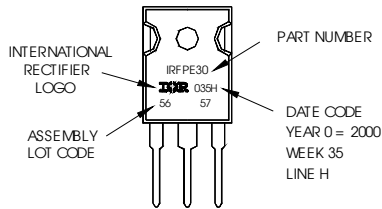
TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
 WITH ASSEMBLY
 LOT CODE 5667
 ASSEMBLED ON WW 35, 2000
 IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line
 position indicates "Lead-Free"



Data and specifications subject to change without notice.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>