

## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	- 200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V   3.0
$Q_g$ (Max.) (nC)	11
$Q_{gs}$ (nC)	7.0
$Q_{gd}$ (nC)	4.0
Configuration	Single

### FEATURES

- Dynamic  $dV/dt$  Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

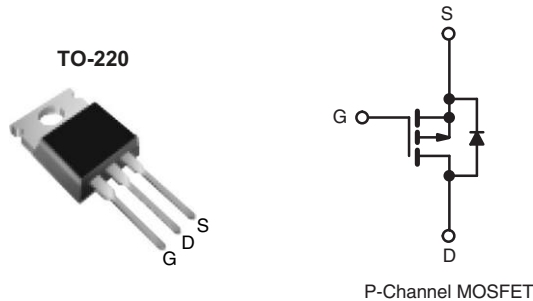


Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

The Power MOSFETs technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRF9610PbF SiHF9610-E3
SnPb	IRF9610 SiHF9610

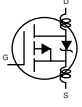
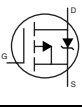
ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		- 200	V
Gate-Source Voltage	$V_{GS}$		$\pm 20$	
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$	- 1.8	A
		$T_C = 100$	- 1.0	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		- 7.0	
Linear Derating Factor			0.16	W/°C
Maximum Power Dissipation	$T_C = 25$ °C		$P_D$	20
Inductive Current, Clamp	$I_{LM}$		- 7.0	A
Peak Diode Recovery $dV/dt^c$	$dV/dt$		- 5.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw		10	
			1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).
- Not applicable.
- $I_{SD} \leq -1.8$  A,  $dI/dt \leq 70$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

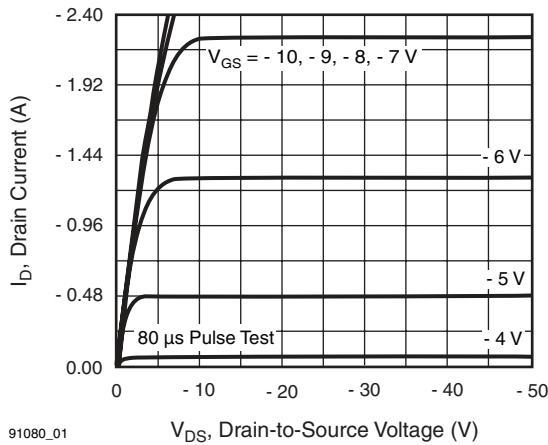
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	6.4	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		- 200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	- 0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$		-	-	- 100	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.90\text{ A}^b$	-	-	3.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -0.90\text{ A}^b$		0.90	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 10		-	170	-	pF
Output Capacitance	$C_{oss}$			-	50	-	
Reverse Transfer Capacitance	$C_{rss}$			-	15	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -3.5\text{ A}, V_{DS} = -160\text{ V},$ see fig. 11 and 18 <sup>b</sup>	-	-	11	nC
Gate-Source Charge	$Q_{gs}$			-	-	7.0	
Gate-Drain Charge	$Q_{gd}$			-	-	4.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\text{ V}, I_D = -0.90\text{ A},$ $R_G = 50\text{ }\Omega, R_D = 110\text{ }\Omega$ , see fig. 17 <sup>b</sup>		-	8.0	-	ns
Rise Time	$t_r$			-	15	-	
Turn-Off Delay Time	$t_{d(off)}$			-	10	-	
Fall Time	$t_f$			-	8.0	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.8	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 7.0	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.8\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	- 5.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	240	360	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	1.7	2.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

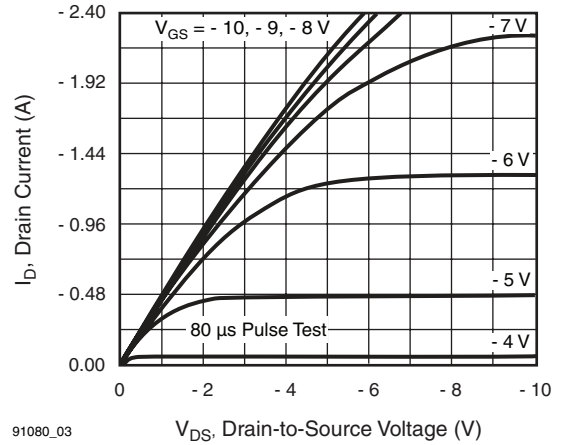
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 5).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

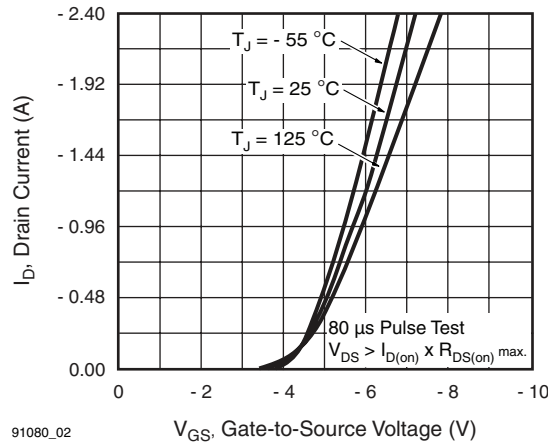
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



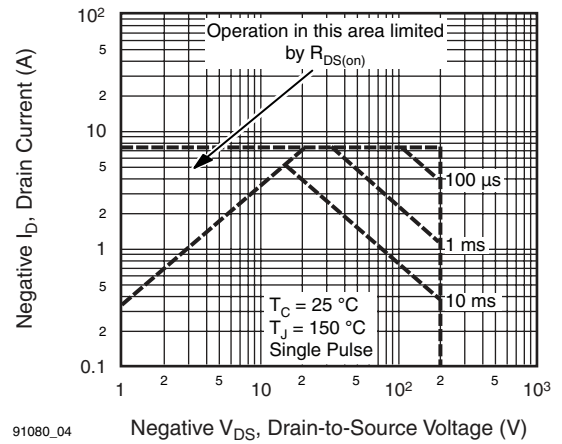
**Fig. 1 - Typical Output Characteristics**



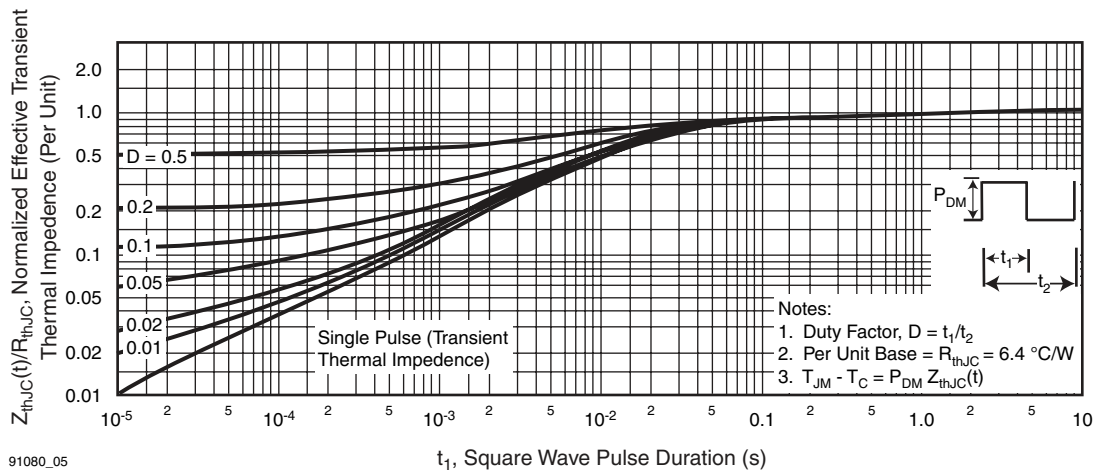
**Fig. 3 - Typical Saturation Characteristics**



**Fig. 2 - Typical Transfer Characteristics**



**Fig. 4 - Maximum Safe Operating Area**



**Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration**



91080\_06 **Fig. 6 - Typical Transconductance vs. Drain Current**



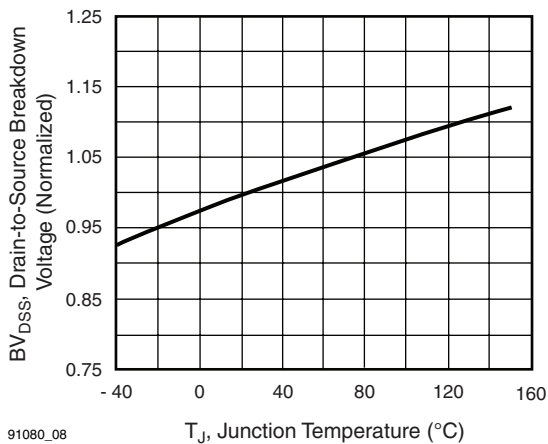
91080\_09 **Fig. 9 - Normalized On-Resistance vs. Temperature**



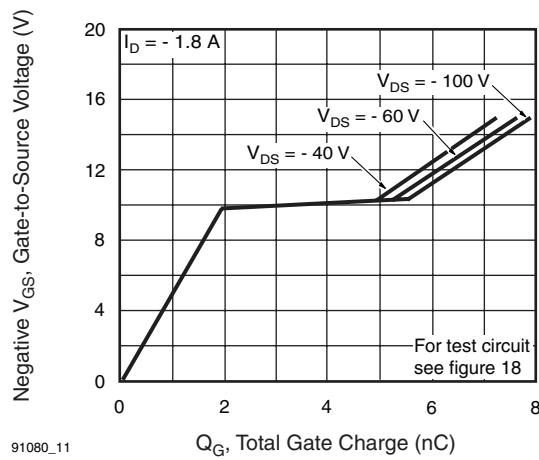
91080\_07 **Fig. 7 - Typical Source-Drain Diode Forward Voltage**



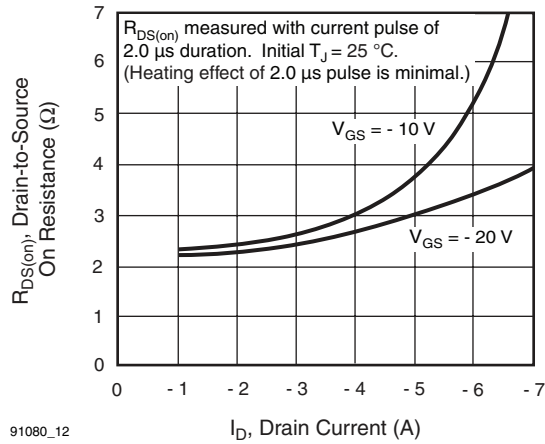
91080\_10 **Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage**



91080\_08 **Fig. 8 - Breakdown Voltage vs. Temperature**

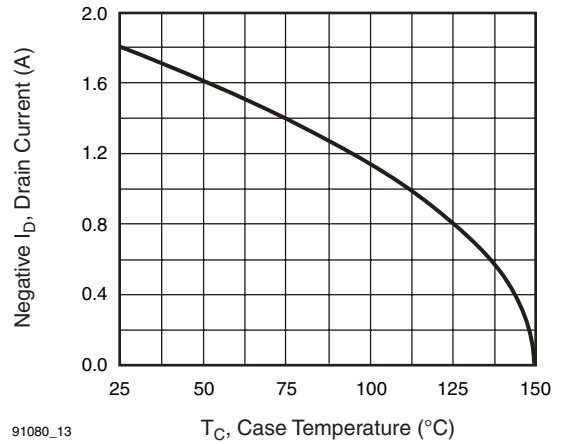


91080\_11 **Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage**



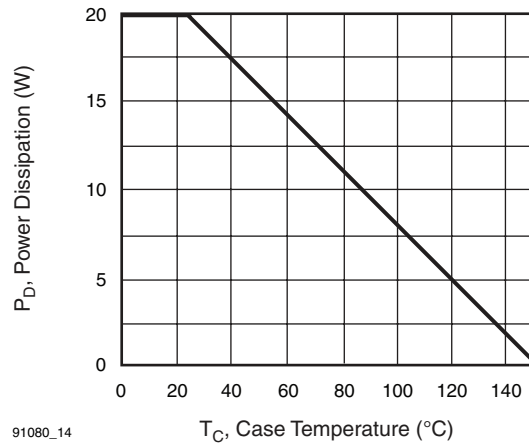
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**Fig. 12 - Typical On-Resistance vs. Drain Current**



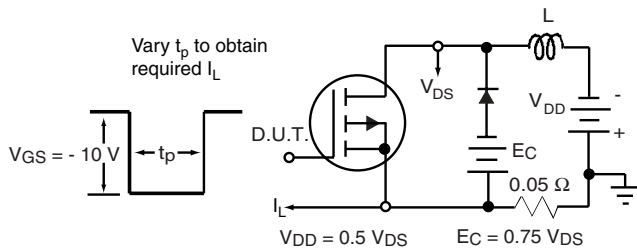
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**Fig. 13 - Maximum Drain Current vs. Case Temperature**

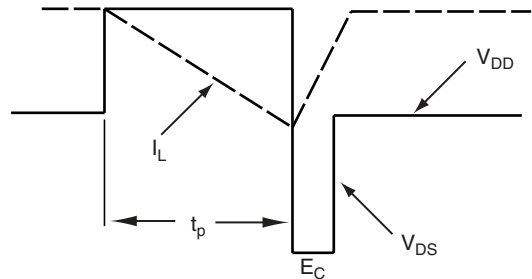


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**Fig. 14 - Power vs. Temperature Derating Curve**



**Fig. 15 - Clamped Inductive Test Circuit**



**Fig. 16 - Clamped Inductive Waveforms**

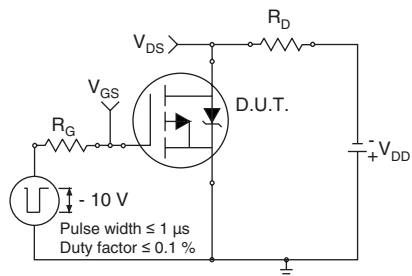


Fig. 17a - Switching Time Test Circuit

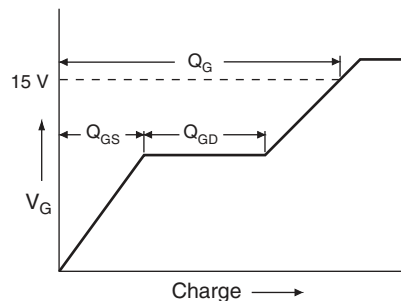


Fig. 18a - Basic Gate Charge Waveform

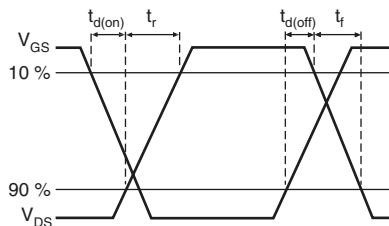


Fig. 17b - Switching Time Waveforms

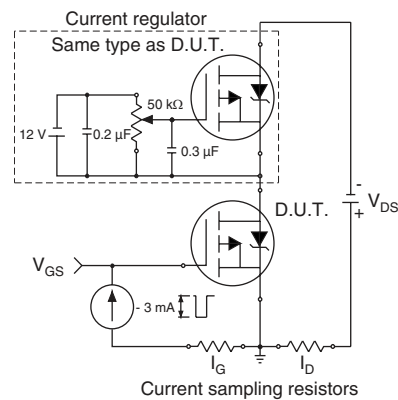
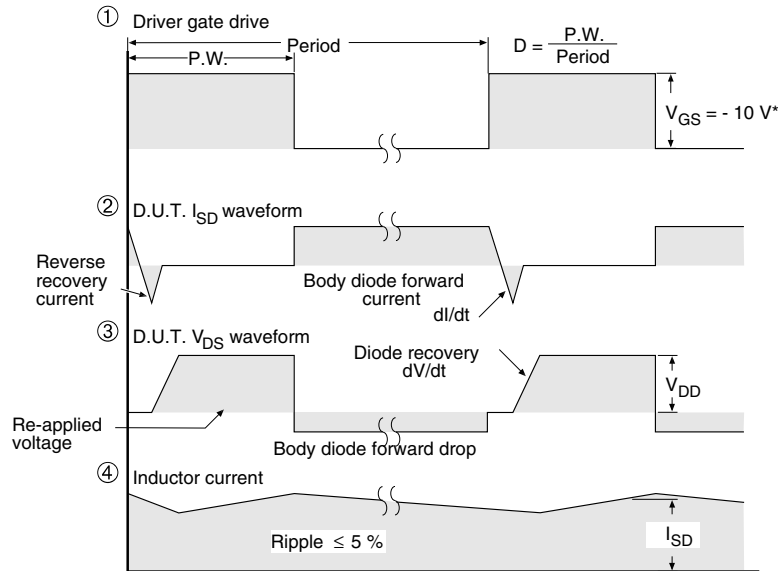
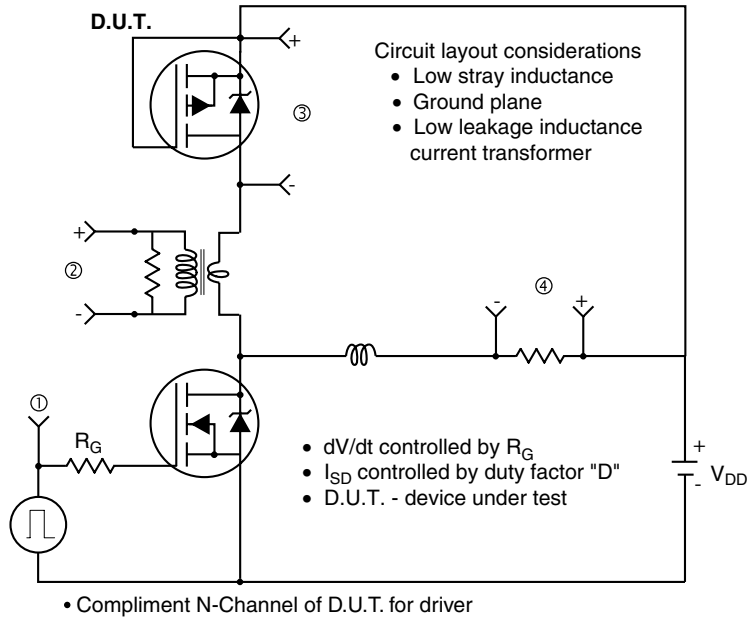


Fig. 18b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = -5\text{ V}$  for logic level and  $-3\text{ V}$  drive devices

**Fig. 19 - For P-Channel**

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