DISPLAY Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128064I ADX-PW-N

Product Specification *Version: 1*

17.06.2017

GENERAL SPECIFICATION

MODULE NO. :

DEM 128064I ADX-PW-N

CUSTOMER P/N:

Version NO.	Change Description	Date
0	Original Version	15.06.2017
1	Change the LCD to Transmissive negative and change the OP./ST. Temperature	17.06.2017

PREPARED BY: GJJ DATE: 17.06.2017

APPROVED BY: MH DATE: 17.06.2017

CONTENTS

1. FUNCTIONS & FEATURES

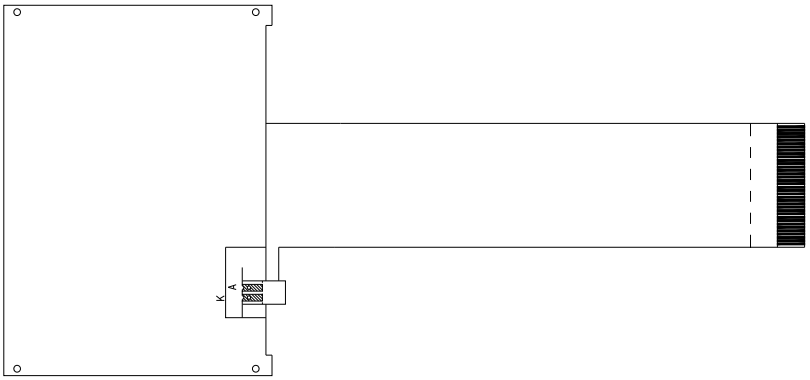
MODULE NAME	LCD Type	Remark
DEM 128064I ADX-PW-N	ASTN Transmissive Negative Mode	

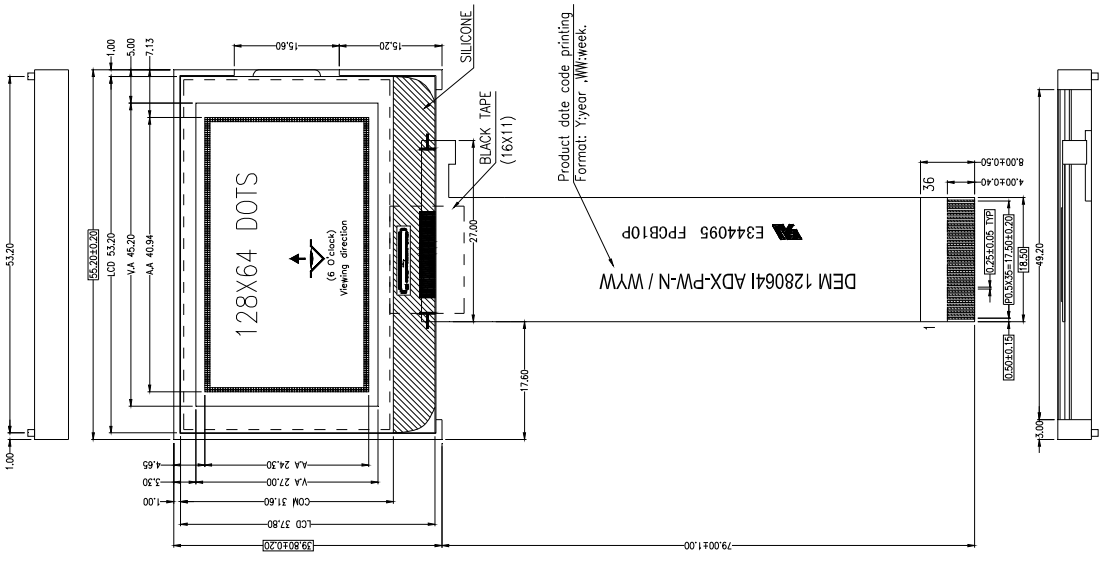
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/65 Duty Cycle, 1/9 Bias
- Power Supply Voltage : 3.3 Volt (typ.)
- LCD Operation Voltage(V0-VSS) : 9.0 Volt (typ.)
- Driver IC : ST7565P (Sitronix)
- Display Format : 128 x 64 Dots
- Interface : Parallel & Serial
- RoHS Compliant

2. MECHANICAL SPECIFICATIONS

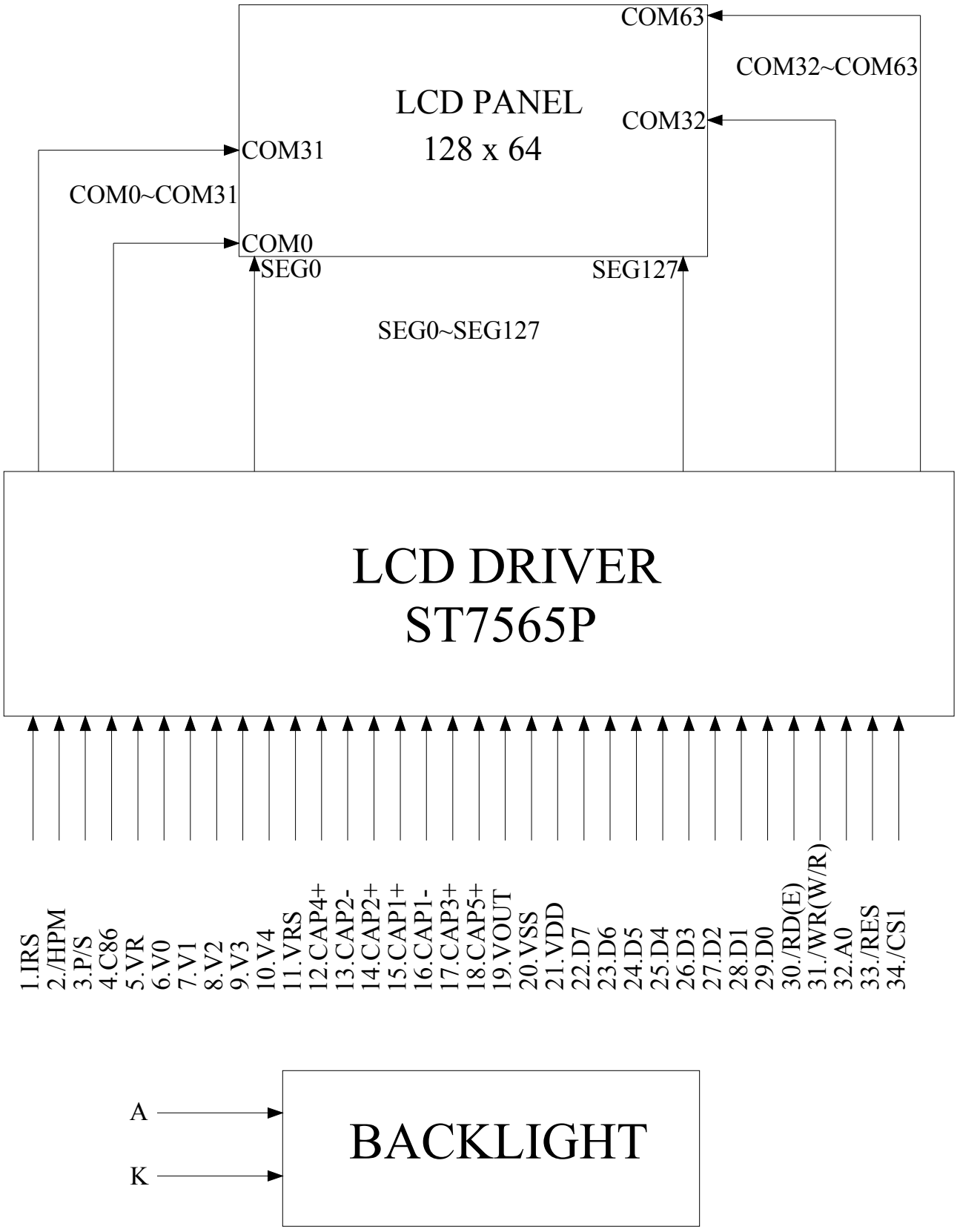
- Module Size (Without FPC) : 55.20 x 39.80 x 5.00 mm
- View Area : 45.20 x 27.00 mm
- Active Area : 40.94 x 24.30 mm
- Dot Size : 0.30 x 0.36 mm
- Dot Pitch : 0.32 x 0.38 mm
- Dot Gap : 0.02 mm

3. EXTERNAL DIMENSIONS (unit: mm)





4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

<table>
<tr><th>Pin No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>IRS</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is
regulated by an external resistive voltage divider attached to the VR terminal</td></tr>
<tr><td>2</td><td>/HPM</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode</td></tr>
<tr><td>3</td><td>P/S</td><td>This pin configures the interface to be parallel mode or serial mode.
P/S = “H”: Parallel data input/output.
P/S = “L”: Serial data input.
When P/S = “L”, D0 to D5 must be fixed to “H”./RD (E) and /WR (R/W) are fixed to either “H” or “L”.</td></tr>
<tr><td>4</td><td>C86</td><td>This is the MPU interface selection pin.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 Series MPU interface.</td></tr>
<tr><td>5</td><td>VR</td><td>Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider.
IRS = “L” : the V0 voltage regulator internal resistors are not used.
IRS = “H” : the V0 voltage regulator internal resistors are used.</td></tr>
<tr><td>6</td><td>V0</td><td rowspan="5">This is multi-level power supply for liquid crystal drive.
Voltage levels are determined based on VDD, and must maintain the relative magnitudes show below.
V0>=V1>=V2>=V3>=V4>=VSS
Master operation when the power supply turns on, the internal power supply circuits produce V1 to V4 voltage shown below. The voltage setting are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr>
<tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr>
<tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr>
<tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr>
</table></td></tr>
<tr><td>7</td><td>V1</td></tr>
<tr><td>8</td><td>V2</td></tr>
<tr><td>9</td><td>V3</td></tr>
<tr><td>10</td><td>V4</td></tr>
<tr><td>11</td><td>VRS</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td></tr>
<tr><td>12</td><td>CAP4+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.</td></tr>
<tr><td>13</td><td>CAP2-</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP2+ terminal.</td></tr>
<tr><td>14</td><td>CAP2+</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP2- terminal.</td></tr>
<tr><td>15</td><td>CAP1+</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP1- terminal.</td></tr>
<tr><td>16</td><td>CAP1-</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP1+ terminal.</td></tr>
<tr><td>17</td><td>CAP3+</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and CAP1- terminal.</td></tr>
<tr><td>18</td><td>CAP5+</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.</td></tr>
<tr><td>19</td><td>VOUT</td><td>DC/DC voltage converter. Connects a capacitor between this terminal and VSS or VDD</td></tr>
</table>

		terminal.
20	VSS	Ground
21	VDD	Power supply
22	D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface (SPI-4) is selected (P/S = "L") : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 should be connected to VDD or floating. When the chip select is not active, D0 to D7 are set to high impedance.
23	D6	
24	D5	
25	D4	
26	D3	
27	D2	
28	D1	
29	D0	
30	/RD (E)	• When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L". • When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
31	/WR (R/W)	• When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type : When R/W = "H": Read. When R/W = "L": Write.
32	A0	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0="HIGH": indicates that D0 to D7 are display data. A0=":LOW": indicates that D0 to D7 are control data.
33	/RES	When /RES is set to LOW, the settings are initialed. The reset operation is performed by the /RES signal level.
34	/CS1	This is the chip select signal for first chip. when /CS1=LOW, the chip select becomes active and the data/commands I/O is enabled
35	K	LED-
36	A	LED+

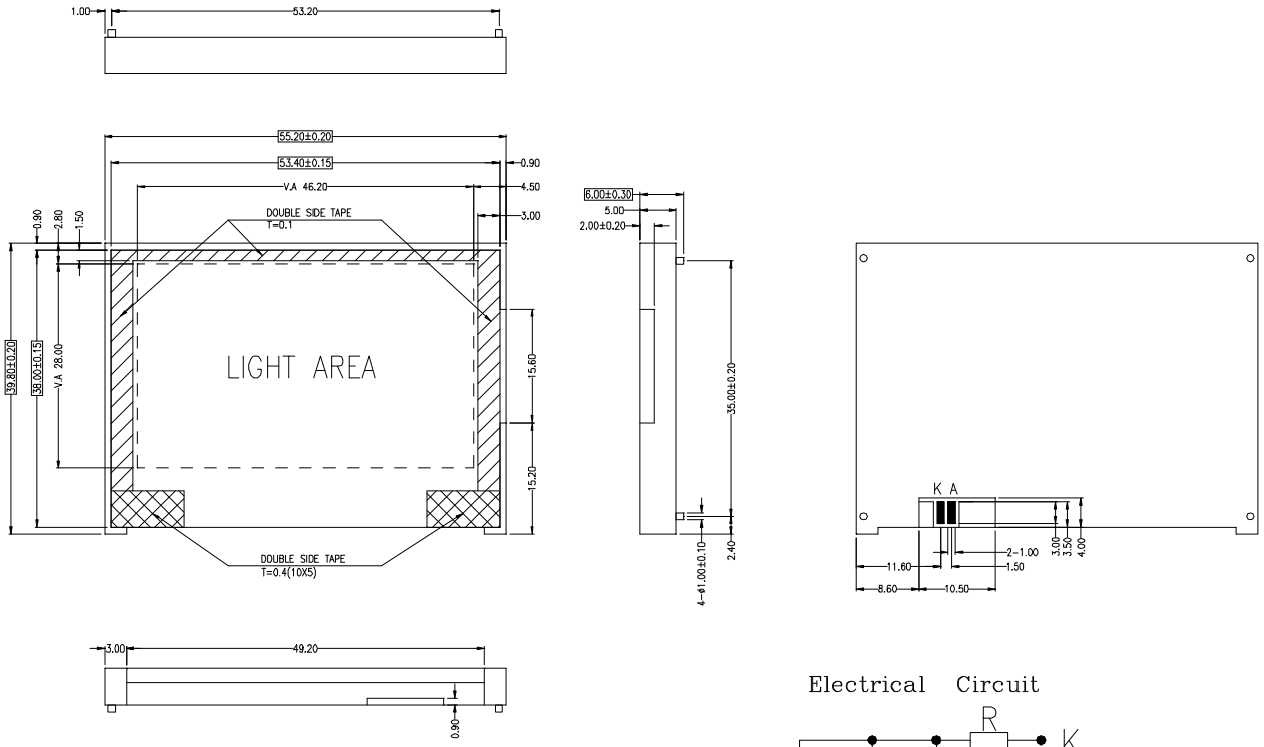
6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD	0.3 ~ 3.6	V
Power Supply Voltage (VDD standard)	VDD2	0.3 ~ 3.6	V
Power Supply Voltage (VDD standard)	V0, VOUT	0.3 ~ 14.5	V
Power Supply Voltage (VDD standard)	V1, V2, V3, V4	V0 to 0.3	V
Operating Temperature	Topr	–30 to +80	°C
Storage Temperature	Tstr	–40 to +90	°C

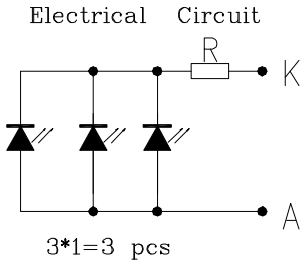
7. BACKLIGHT ELECTRONICS/OPTICAL SPECIFICATIONS

Electronics/Optical Specifications: (Color: White)

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V_f	--	3.1	--	V	
Forward Current	I_f	--	45	60	mA	V_f=3.1V
Power Dissipation	P_d	--	--	0.21	W	V_f=3.1V
Reverse Voltage	V_R	--	--	5	V	--
Reverse Current	I_R	--	--	0.1	mA	V_r=5V
Luminous Intensity	Lv	800	--	--	cd/m^2	V_f=3.1V
Luminous Uniformity	Avg	70	--	--	%	V_f=3.1V
Color Chromaticity	X	0.26	--	0.33	--	fl=20mA Ta=25℃ Each chip
	Y	0.26	--	0.33	--	



Remarks:
1.Unmarked tolerance is ±0.3
2.All materials comply with RoHs
3. ▭ ...:critical dimension.
4.COLOR:WHITE
5.Life time 50,000 hours



8. DC CHARACTERISTICS

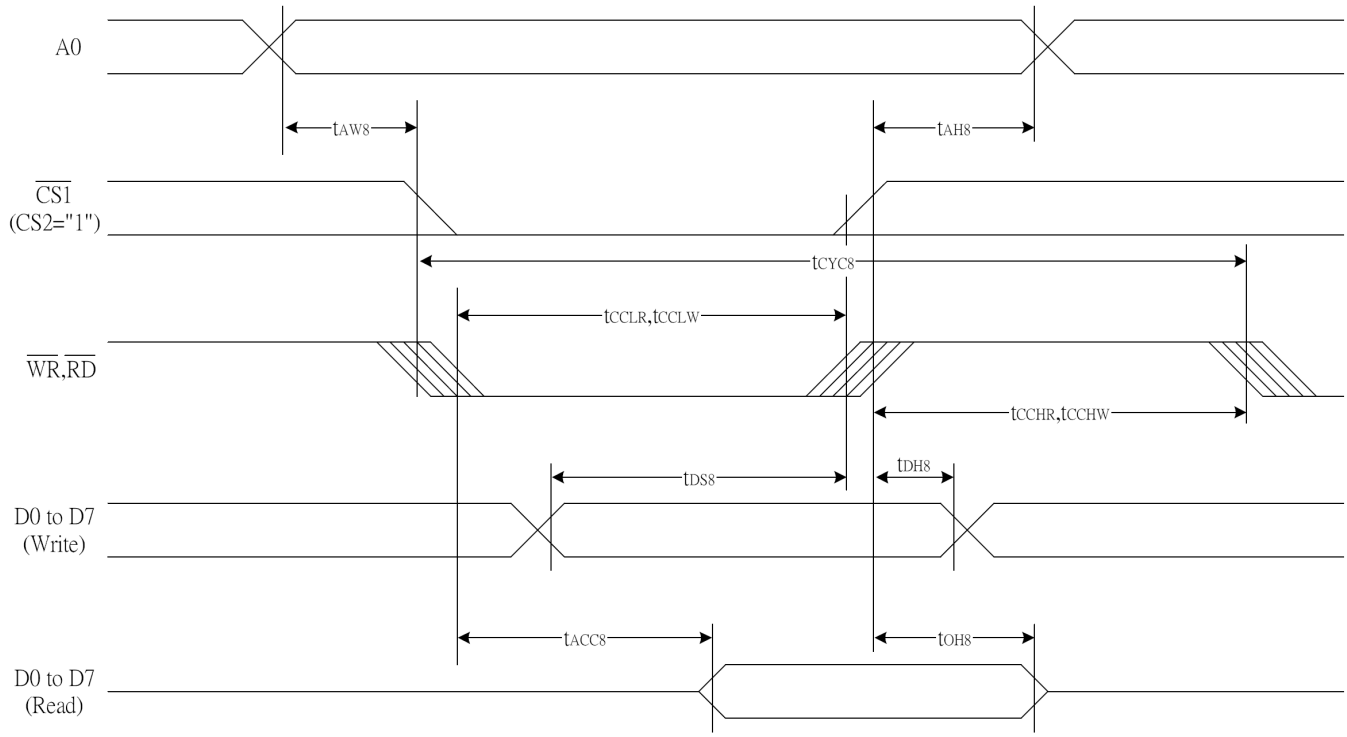
Item	Symbol	Standard Value			Test Condition	Unit
		Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	3.0	3.3	3.6		V
Operating Voltage	V_{LCD}	8.7	9.0	9.3	V0-V_{SS}	
Current Consumption	I_{DD}	---	170	255		uA

9. AC ELECTRICAL CHARACTERISTICS

9.1 System bus READ/WRITE characteristics for the 8080 series MPU

(VDD=3.3V, VSS=0V)

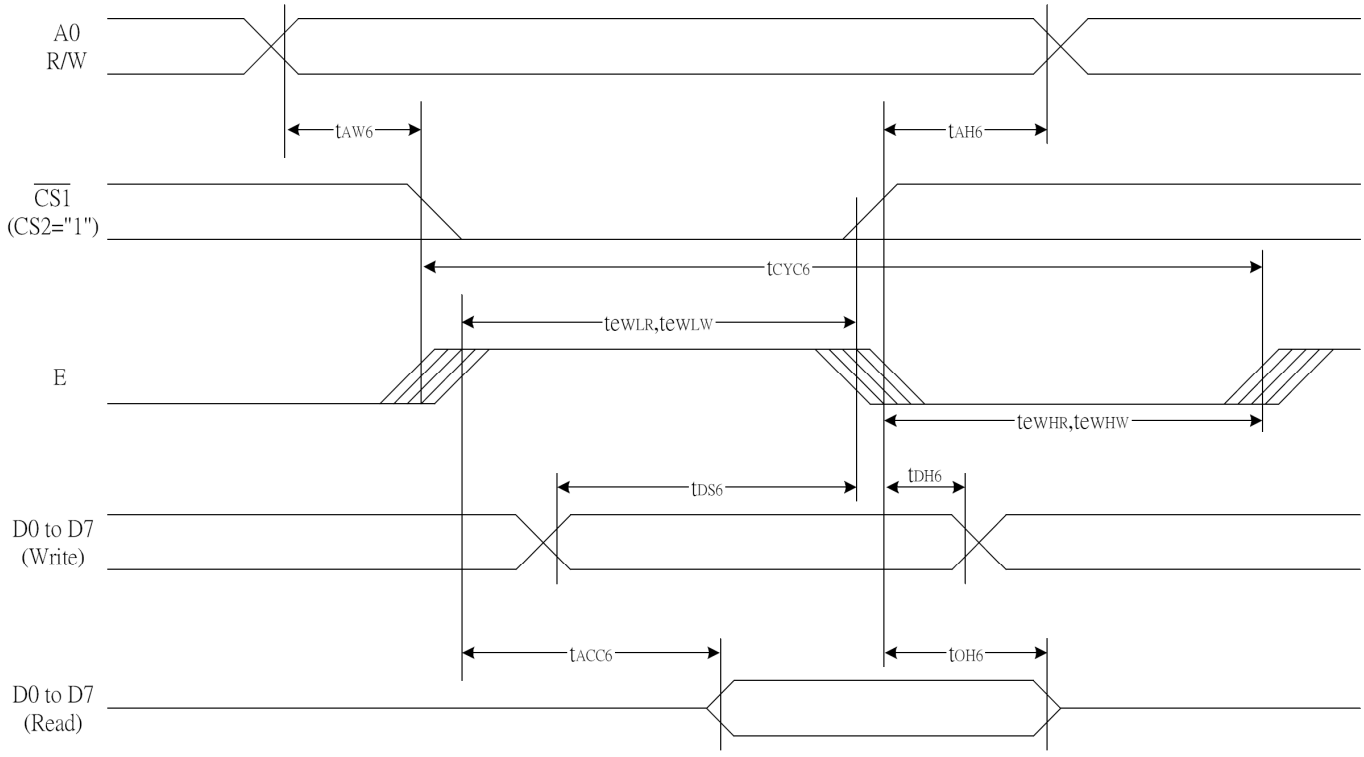
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	CL = 100 pF	—	70	
READ Output disable time		t_{OH8}	CL = 100 pF	5	50	



9.2 System bus READ/WRITE characteristics for the 6800 series MPU

(VDD=3.3V, VSS=0V)

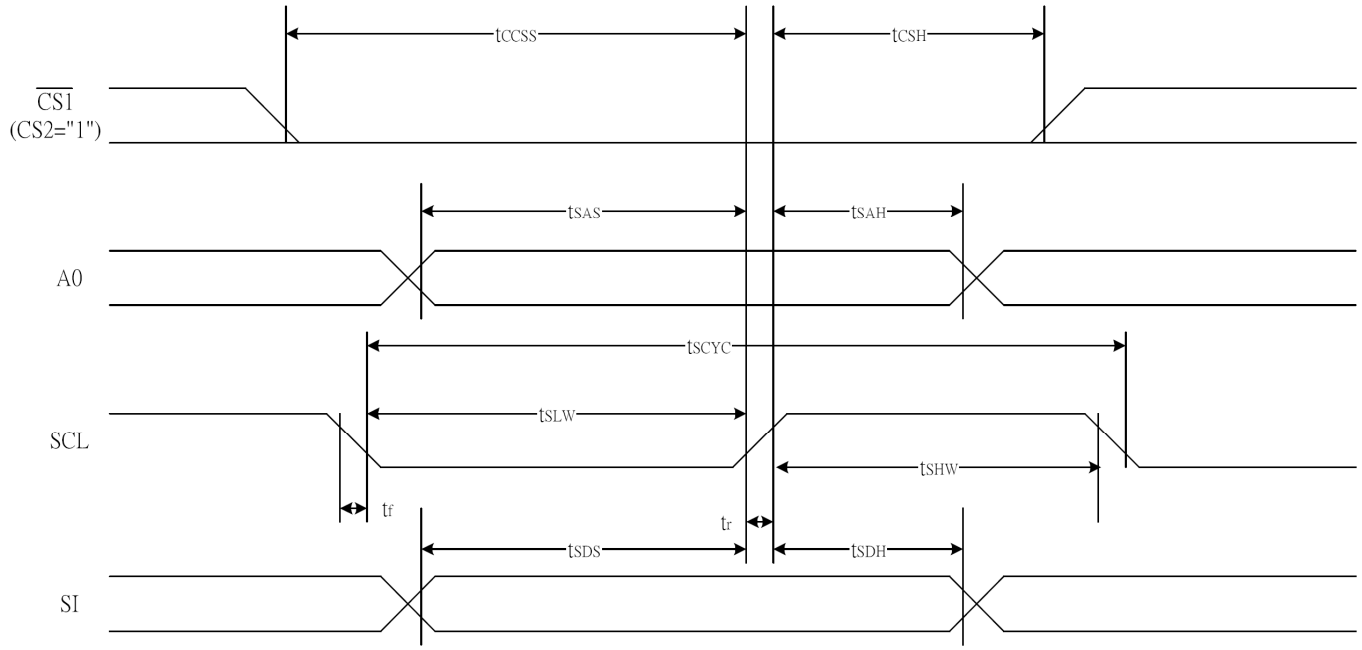
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	CL = 100 pF	—	70	
READ Output disable time		t_{OH6}	CL = 100 pF	5	50	



9.3 The Serial Interface

(VDD=3.3V,VSS=0V)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		50	—	ns
SCL "H" pulse width		t_{SHW}		25	—	
SCL "L" pulse width		t_{SLW}		25	—	
Address setup time	A0	t_{SAS}		20	—	
Address hold time		t_{SAH}		10	—	
Data setup time	SI	t_{SDS}		20	—	
Data hold time		t_{SDH}		10	—	
CS-SCL time	CS	t_{CSS}		20	—	
CS-SCL time		t_{CSH}		40	—	



10. COMMAND TABLE

(Note) *: disabled data

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

11. ACCEPT QUALITY LEVEL (AQL)

11.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.
11.2 Inspection Plan: MIL-STD-105E, Normal Inspection Level II, Single Sampling Plan.

12. RELIABILITY TEST

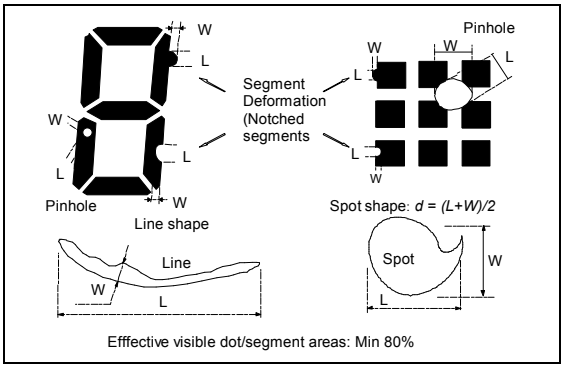
Operating life time: 50,000 hours (at room temperature without direct irradiation of sunlight)
Reliability characteristics shall meet following requirements.

Test Item	Test Condition
High temperature storage	+90□ x 96hrs
Low temperature storage	-40□ x 96hrs
High temperature operation	+80□ x 96hrs
Low temperature operation	-30□ x 96hrs
High temperature, High humidity	+60□ x 90%RH x 96hrs
Thermal shock	-30□ x 30min→ +25□ x10s →+80□ x 30min 5Cycles
Vibration test	Frequency xSwing xTime 40Hz x4mm x4hrs
Drop test	Drop height xNo. of drops 1.0m x6drops

13. QUALITY DESCRIPTION

DEFECT SPECIFICATION:

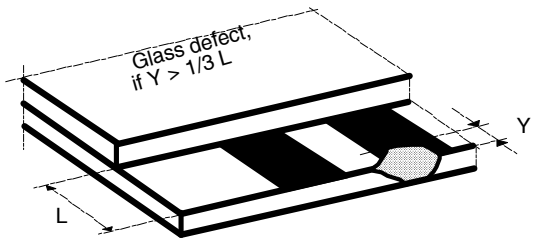
a: Table for Cosmetic defects
(Note: nc = not counted).
Sizes and number of defects
(Max. Qty)



Defect Type	Max. defect size [µm] d or L W	Max. Quantity.
Black or White Spots	d ≤ 100	nc
	150< d ≤ 300	3
Black or White Lines	W ≤ 10	nc
	L ≤ 3000 W ≤ 30	2
	L ≤ 2000 W ≤ 50	2
Pinhole	d ≤ 100 150< d ≤ 300	nc 1/segment
(Total defects)		(5)
Segment Deformation	W ≤ 100	nc
Bubble (e.g. under pola)	d ≤ 150	nc
	200< d ≤ 400	2

Examples/ Shapes

b: Glass defects
b1:Glass defects at contact ledge



b2:Glass chipping in other areas shall not be in conflict with the product's function.

14. LCD MODULES HANDLING PRECAUTIONS

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0□). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

15. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections